7-1-1994

Silicon-on-insulator MOSFETS: Material, process and device characteristics

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Silicon-on-Insulator MOSFETS: Material, Process, and Device Characteristics

by

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A Thesis Submitted

in

Partial Fulfillment

of the

Requirements for the Degree of

MASTER OF SCIENCE

in

Electrical Engineering

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ROCHESTER, NEW YORK

JULY, 1994

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Acknowledgments

I would like to thank Dr. S.S. Iyer from IBM for working with us to produce the bonded and etched-back SOI substrates. Without him, this project would not have been possible.

I am very thankful for the support of my thesis committee: Dr. I. R. Turkman for his seemingly endless knowledge of device operation, Dr. L. F Fuller for both his process and device-related insight and financial support, and Dr. S. K. Kurinec, my advisor, for her council on nearly every aspect of this project. In addition, I would like to thank S. Blondel, T. Griswald and G. Runkle for keeping the fab, metrology, and analytical equipment running so that I could complete this project. Finally, I would like to thank my wife, Bonnie, for her unending support and love.

Abstract

NMOS and PMOS Single-crystal-silicon-on-insulator (SOI) MOSFETs have been fabricated at RIT using a Bonded and Etched-back process for substrate formation. A test chip, containing inverters, contact and sheet resistance structures, and various NMOS and PMOS transistors, was fabricated on a 2000Å SOI substrate formed by a Bonded and Etched-back technique. Effective mobilities, subthreshold swings, and threshold voltages of the fabricated devices were extracted to investigate the impact of a Bonded and Etched-back process on device performance. A hole mobility of 486 $cm^2/V\text{-}s$ was obtained in PMOS SOI, comparable to state-of-the-art, and exceeding any mobility previously reported at RIT. A subthreshold swing of 110mV/decade was observed in PMOS SOI. The NMOS devices were found to be inferior to those fabricated external to RIT using this SOI process. It was found that hole mobility increased by 14% on average and electron mobility increased by 6% on average for SOI devices compared to similar conventional devices fabricated in bulk silicon. Subthreshold swing decreased 93% on average for SOI devices compared to conventional bulk-silicon devices. SOI is identified as an attractive process, having significant performance advantages over bulk-silicon devices.

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Table of Symbols

SOI ..... Silicon-on-Insulator

B-E ..... Bonded and Etched-Back

μ ..... Mobility

SS, S/S ..... Subthreshold Swing

SIMOX ..... Separation by IMplanted OXygen

LOCOS ..... LOCal Oxidation Of Si

DIBL ..... Drain-Induced Barrier Lowering

ε_x ..... Electric Field in X-Direction

G_m ..... Transconductance

Φ ..... Work Function

SOS ..... Silicon-on-Sapphire

ZMR ..... Zone-Melting Recrystallization

SEU ..... Single-Event Upset

X_j ..... Junction Depth

POLY ..... Polysilicon

BOE ..... Buffered Oxide Etch

RIE ..... Reactive Ion Etch

LTO ..... Low-Temperature Oxide

sccm ..... Standard Cubic Centimeters per Minuite

Slm ..... Standard Liters per Minuite

Chapter 1 Introduction

Today, CMOS integrated circuits are fabricated almost exclusively on bulk silicon substrates for two well-known reasons: electronic grade material produced either by the Czochralski or floating zone technique is readily available, and a high-quality oxide can easily be grown on silicon. However, modern MOSFETs made in bulk silicon are far from ideal structures. Conventional architectures fabricated in bulk silicon are degraded by device parasitics, and short-channel effects limit the degree to which they can be scaled down. Engineering new ways to get around these problems is becoming more difficult and results in complex processes and lower yields.

One technology which has shown much promise in avoiding the problems associated with silicon devices, is Silicon-on-Insulator (SOI). The SOI structure contains a thin film of single-crystal silicon on top of an insulating substrate, typically silicon dioxide [1]. Shown in Figure 1.1, the basic SOI structure has demonstrated a number of processing advantages as well as many significant performance advantages. In addition, SOI has also tackled some of the problems of down-scaling. Process, performance, and sizing advantages are the three major factors driving SOI technology.

The type of Silicon-on-Insulator material and technology currently being used varies for specific applications. Some SOI technologies are suitable for Power and high-voltage devices, while others exhibit high speeds [2]. Some lend themselves to 3-D integration, and others, to radiation hardness. To date no single technology has proven to demonstrated all desirable features; however, two do show considerable promise: the SIMOX (Separation by IMplanted OXygen) process, and, more recently, the Bonded and Etched-Back (B-E) process.

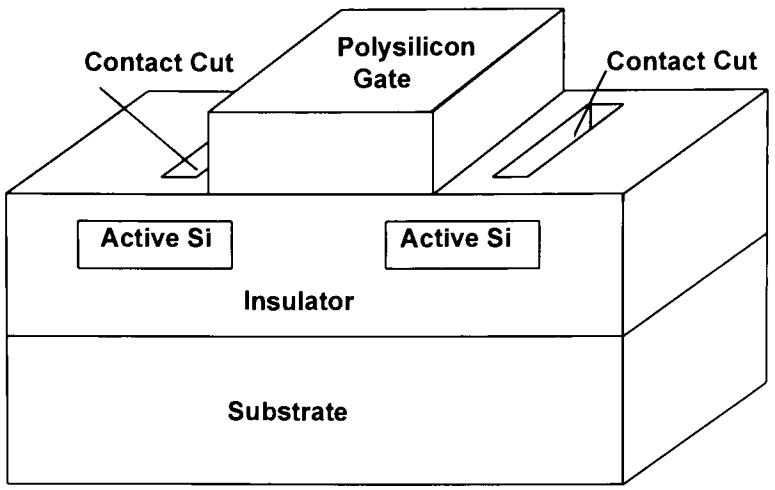

Figure 1.1: Basic SOI Structure

Although Silicon-on-Insulator technology has proven advantageous, a number of key issues remain which hinder this non-conventional architecture from being a viable manufacturable alternative. The material-related issues come from the inability to produce thin-film silicon uniformly and with low defect densities [3]. Device-related obstacles involve the underlying oxide and its important influence on device behavior such as threshold voltage, off-state leakage, and punch-through [1]. Advances in SOI technology, including the work herein, address these problems and offer solutions which identify SOI as a viable alternative, having significant performance advantages over bulk silicon-devices.

Chapter 2 Factors Driving SOI Technology

The factors driving Silicon-on-Insulator technology fall primarily into three categories: scaling limitations in conventional architectures, SOI process advantages, and SOI device performance advantages. Scaling limitations include those imposed by CMOS packing densities, device parasitics, and high electric fields. SOI process advantages include lowered implant energies, a reduction in topography, and the elimination of vertical "contact spiking" Improved mobility, transconductance, and subthreshold slope, along with reduced lateral electric field and reduced Drain-Induced Barrier Lowering (DIBL) are among the SOI device performance advantages. Together, these factors drive advances to make SOI a viable production process.

2.1 SOI and the Scaling Limitations in Conventional Architectures

Submicron scaling of CMOS devices has necessitated sophisticated process and structural enhancements to meet performance, packing density, and reliability goals. The entire CMOS process flow is affected, including device design, isolation processes, starting material, and multilevel interconnect technologies. High-speed transistor designs, in particular, are being driven by the need for embedded logic and microprocessor chips able to operate at clock speeds approaching 500 MHz, while dissipating very low power [4].

As technology drives towards .35um feature sizes, structural innovations such as ultrathin silicon-on-insulator (SOI) are emerging as viable alternatives due to their inherent speed and isolation advantages, as well as their simplified manufacturing process. These advantages also translate to improved cost, assuming SOI manufacturing yields become comparable to those of bulk silicon.

2.1.1 CMOS Packing Density

Using conventional architectures, CMOS packing density has been limited by isolation processes like LOCOS (LOCal Oxidation of Silicon) (Figure 2.1.1) [5]. This technique places tight constraints on inter-well (n+ to p+ spacing) and intra-well design rules due to active area encroachment and field oxide thinning, especially when considering submicron features. Even the more recent non-LOCOS isolation techniques such as trench/refill (Figure 2.1.2) and Selective Epitaxial Growth (SEG) have been unsuccessful in replacing LOCOS because of their increased process complexity and variability [5-7].

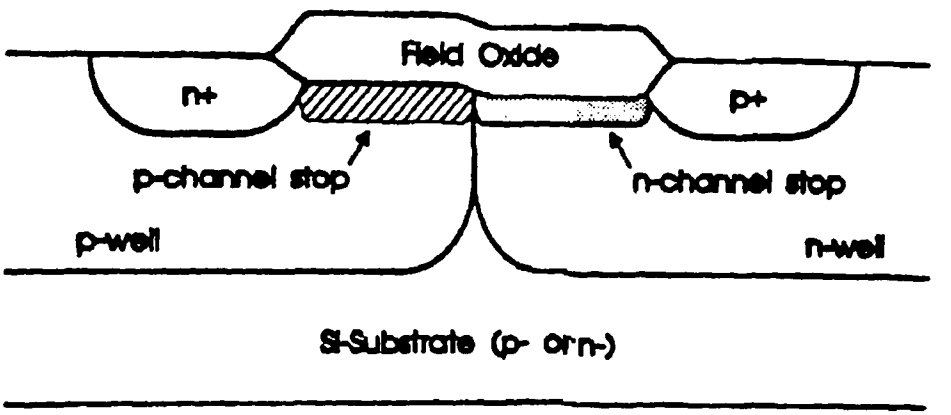

Figure 2.1.1: LOCOS

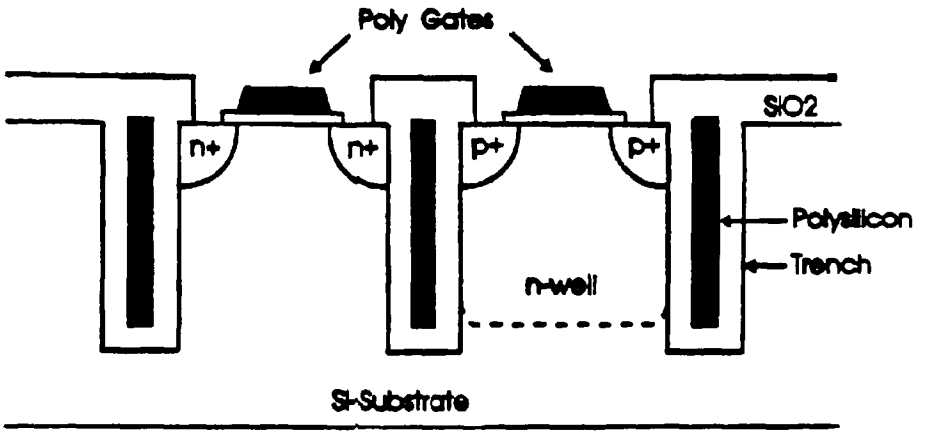

Figure 2.1.2: Trench Refill

The ultrathin SOI structure offers a solution to most of the transistor and isolation design limitations encountered when scaling conventional architectures to the submicron regime. Figure 2.1.3 presents a comparison of a conventional twin-well, LOCOS-isolated, CMOS bulk-silicon structure with a mesa-isolated, equivalent SOI structure [1]. The SOI structure reduces the inter-well design rules dramatically. CMOS SOI isolation techniques improve packing density by almost 40 percent compared to bulk CMOS [4]. This offers a simple, cost-effective solution to the ever-present problem of trying to fit more in a smaller space.

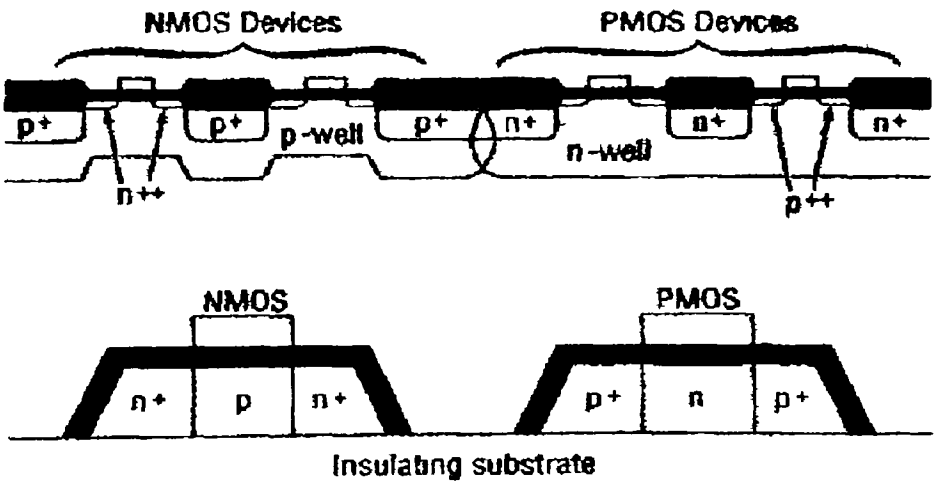

Figure 2.1.3: Comparison of LOCOS Twin-Well with SOI-Equivalent

2.1.2 Device Parasitics

Bulk MOSFETs are made in silicon wafers having a thickness of approximately 500 micrometers, but only the first micron at the top of the wafer is used for device fabrication. Interactions between devices and the substrate cause a range of parasitic effects. One such effect is the parasitic capacitance between diffused active regions and the substrate. This capacitance increases with substrate doping, and becomes more significant in modern submicron devices where the dopant in the substrate is higher to counteract short-channel effects [8]. The source and drain capacitance consists not only of the depletion regions associated with the junctions, but also the capacitance between the junction and the heavily-doped channel-stop region located under the field oxide. Latch-up, as illustrated in Figure 2.1.4, is another unwanted parasitic effect found in CMOS devices [5,8]. Latch-up is the unwanted triggering of an npnp thyristor structure, inherently present in all bulk-silicon CMOS structures. It becomes a significant problem in devices with small feature sizes, where the gain of the parasitic thyristor bipolar devices becomes large. These parasitic components have been reduced for bulk silicon by minimizing the source and drain junction areas and by creating local interconnects and placing contacts over the field area [9]. The latch-up phenomenon can be reduced by epitaxial substrates or by deep trench isolation [10]. However, these techniques necessitate sophisticated processing, which impacts both the yield and the cost of manufacturing.

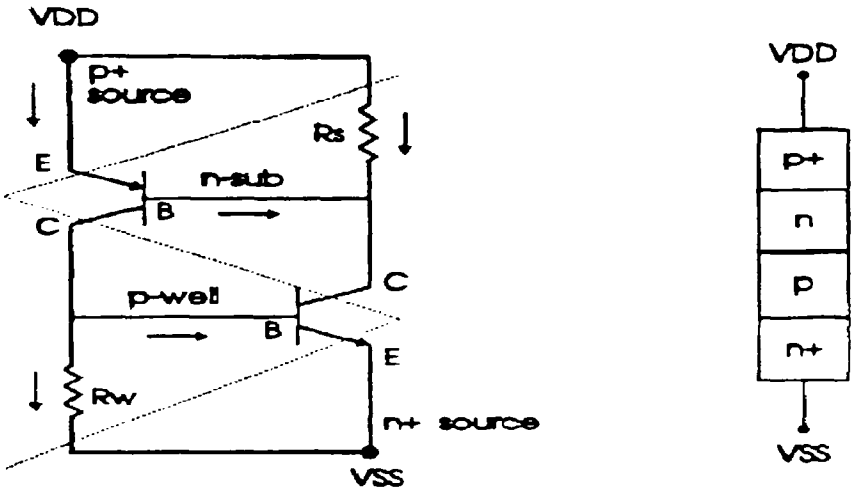

Figure 2.1.4: Figure 2.1.4: Latch-up; npnp Thyristor Structure

If a Silicon-on-Insulator (SOI) substrate is used, quasi-ideal devices can be fabricated. The full dielectric isolation of the devices prevents most of the parasitic effects found in bulk-silicon devices. To illustrate a few, a cross-sectional schematic representation of a bulk-silicon CMOS inverter is shown in Figure 2.1.5 [5]. As indicated earlier, most parasitic effects in bulk-silicon originate in the interaction between the active areas and the substrate of the devices. Latch-up finds its origin in the parasitic npnp structure of the CMOS inverter represented in Figure 2.1.5. The latch-up path can be modeled by two bipolar transistors, formed by the substrate, the well, and the source and drain junctions. Latch-up can be triggered by a number of different mechanisms, such as voltage overshoots, junction avalanching, displacement current, and photocurrents. A necessary condition for latch-up is that the current gain of the loop formed by the two bipolar transistors be larger than 1 ($\beta>1$). In an SOI CMOS inverter, a latch-up path is ruled out because there is no current path to the substrate, and the lateral npnp structures contain heavily-doped bases (P^+ and N^+ drains), which reduce the gain of the bipolar devices to nearly zero.

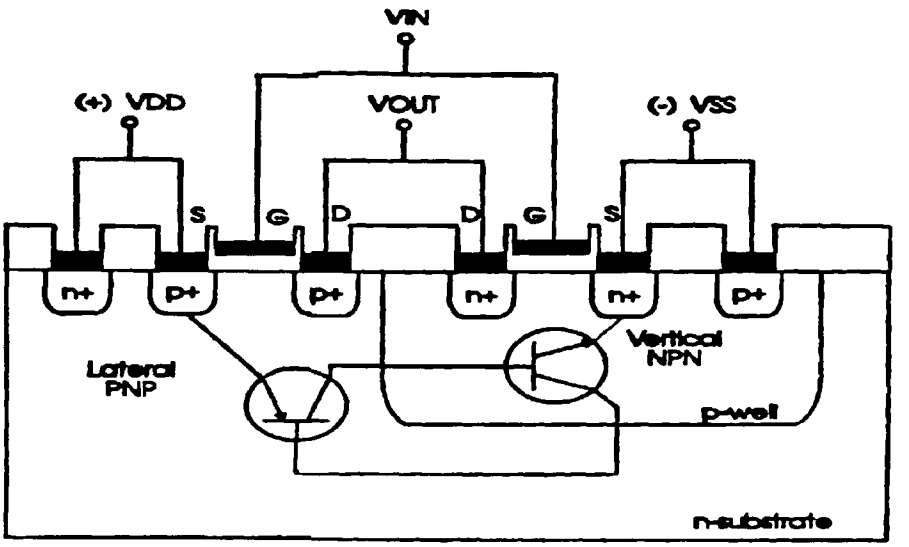

Figure 2.1.5: Latch-up in a Bulk-Silicon CMOS Inverter (Cross-Section)

Bulk-silicon circuits use reversed-biased junctions to isolate devices from one another. Consider, for instance, the drain on the n-channel device of Figure 2.1.5. The drain is always positively biased with respect to the substrate, having a voltage ranging from GND to $+V_{DD}$. Therefore, a depletion capacitance is associated with the drain junction. The maximum capacitance value, which depends on the substrate doping, is reached when the drain bias is zero volts. The higher the dopant concentration is, the higher the capacitance will be.

In SOI devices, on the other hand, the maximum capacitance between junctions and the substrate is the capacitance of the buried insulator (the capacitance tends toward zero if thicker insulators are used). This capacitance is proportional to the dielectric constant of the insulating material. Silicon dioxide, commonly used as a buried insulator, has a dielectric constant of three times smaller than that of silicon ($\varepsilon_{ox}=3.9\varepsilon_o$, $\varepsilon_{si}=11.9\varepsilon_o$). Therefore, a junction which lies on a silicon dioxide layer results in a parasitic capacitance which is three times smaller than that of a bulk-silicon junction, giving rise to a depletion depth equal to the buried silicon dioxide thickness. Because the buried insulator thickness does not need to be scaled down as the device feature size is reduced,

parasitic capacitance does not increase as technology advances, contrary to bulk-silicon devices. In addition, a lightly-doped p-type wafer can be used as the underlying substrate for mechanical support. In this case a depletion layer can be created beneath the insulator, further reducing the junction-to-substrate capacitances.

SOI shows great promise for improved device performance. Based on its design, parasitic capacitances are greatly reduced and latch-up is altogether eliminated. It becomes evident that conventional bulk-silicon architectures will not be able to support the reduction of scale, and some alternative such as SOI will have to be sought.

2.1.3 High Electric Fields

As MOSFETs in bulk silicon shrink and supply voltages are not scaled for constant field, higher dopant concentrations are required to avoid punchthrough; thus, internal electric fields increase. High electric fields lower tranconductance (mobility) and increase hot-carrier-induced threshold degradation and instability. Source/drain series resistance and junction capacitance increase quickly and severely degrade transconductance and switching speed.

A well-designed SOI structure can overcome most of these problems due to its geometrical attributes. In bulk-silicon devices, charge-sharing and drain-induced barrier lowering (DIBL) lead to undesirable short-channel effects which must be counteracted with higher doping concentration in the channel regions (Figure 2.1.6a). By adjusting the SOI film thickness to less than the maximum depletion depth in the channel region, charge-sharing and DIBL effects are greatly reduced [1]. This is attributed to the modified electrostatic field distribution in the vertical direction (Figure 2.1.6b) [1]. Thus, channel doping can be lowered independently of the channel length. With reduced channel doping, the fully-depleted structure further lowers the lateral electric field from drain to source, and thereby reduces the short-channel effects at submicron dimensions. MOSFETs down to 0.3μm have been simulated and experimentally verified in thin-film SOI with very low channel dopings (thus, reduced lateral electric fields) on the order of 10^{14} to 10^{15} cm^{-3} [11-13]. They exhibit excellent short-channel behavior, with a nearly-40-percent-improved transconductance (Gm), and higher drive currents due to increased mobilities. The modified electrostatic field proves to be of significant advantage and results in devices which exhibit increased Gm, reduced junction capacitance, improved subthreshold slope, and reduced hot electron effects.

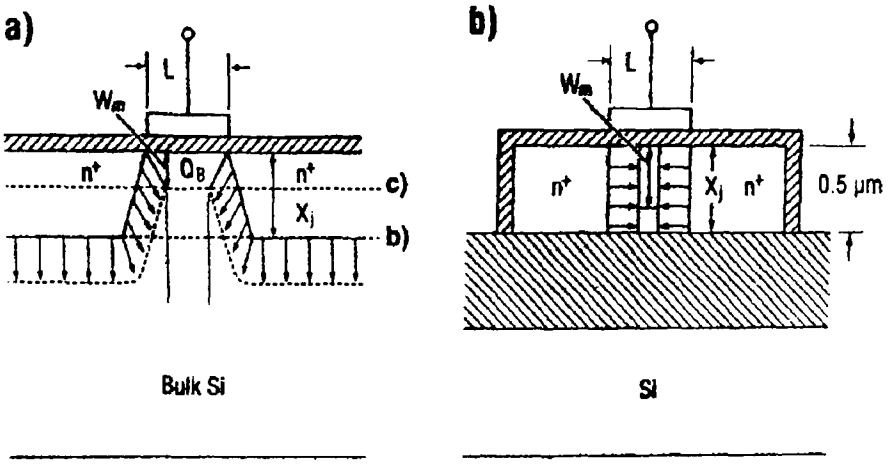

Figure 2.1.6: The Electric Field Distribution in a) Bulk-Silicon MOSFET and b) SOI MOSFET

2.2 Process Advantages

In addition to Silicon-on-Insulator's advantage in overcoming the scaling limitations of conventional architectures, process advantages present strong driving factors as well. In comparison to bulk-silicon CMOS, the SOI process offers more simple steps due to its inherent structure. Among some of the most significant advantages are the lowered implant energies (shallow implants), reduced topography, elimination of vertical contact spiking, and, already mentioned, elimination of LOCOS isolation steps. Reducing the complexity of the process translates to greater savings in cost, and thus adds to the factors driving SOI technology.

2.2.1 Lowered Implant Energies

In thin-film, fully-depleted SOI devices, deep implants are unnecessary. The entire impurity profile in the channel is determined by a single, shallow, and thus low-energy implant. The need for shallower implants leads to greater throughput, which saves money in the manufacturing process. A secondary advantage is that a lower-current implanter can be used in place of a higher one; this too translates to a smaller cost.

2.2.2 Reduction in Topography

In today's complex conventional architectures, vast topographies occur due to various isolation techniques. As the layers build up, it becomes a problem to image and transfer patterns for each following layer, and step coverages become an increasing problem [1]. Elimination of vast topographies requires time-consuming and complex planarization steps, which greatly affect the cycle time and cost of manufacturing.

SOI solves these problems and eliminates the need to perform the complex planarization steps. Because LOCOS isolation is not needed and film thicknesses are very small, no topographical problems with step coverage or pattern imaging/transfer occur. This is a very significant result when considering that conventional processes devote considerable resources in trying to yield that which is inherent to SOI technology.

2.2.3 Elimination of Vertical Contact Spiking

Silicon-on-Insulator CMOS technology also yields other attractive benefits aside from its relatively simple process. Some of the benefits result directly from the SOI structure itself. Shown in Figure 2.2.1 is the formation of a contact to a shallow junction in (A) bulk silicon and in a (B) thin-film SOI [2]. Making a shallow junction is not a trivial task in bulk CMOS. Contact to the shallow junction can be made using a number of materials, including a metal, a silicide, or an alloy. In bulk silicon, unwanted reactions between the junction and the contact material may occur, resulting in situations where the contact material "punches through" the junction. This is common for aluminum contacts (spiking), but also occurs with other metals or silicides, especially along field isolation edges. This phenomenon of junction punch-through leads to high leakage currents.

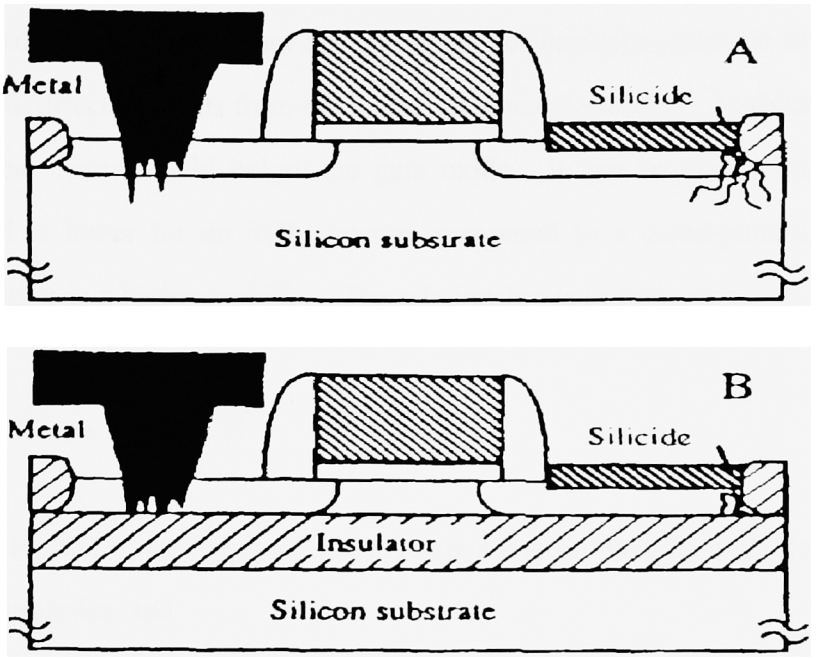

Figure 2.2.1: Formation of a Contact to a Shallow Junction in a) Bulk-Silicon and b) SOI

If, on the other hand, a thin SOI substrate is used, the depth of the junction will be equal to the thickness of the silicon film; the N+ and P+ source and drain junctions would reach and extend to the buried insulator. In this case, there is no junction underneath the metal-silicon contact, and therefore, punch-through caused by a metal-silicon reaction is not possible. This greatly simplifies the sintering process and makes the sintering time less critical.

2.3 Device Performance/Operation Advantages

In addition to the many process advantages that SOI has to offer, a number of very significant device performance advantages exist which truly drive the technology. Among these advantages are increased channel mobilities and improved subthreshold slopes.

2.3.1 Improved Channel Mobility

One of the most significant device-related performance gains for SOI technology, namely speed, directly results from the increased channel mobility. Mobility is a function of the vertical electric field below the gate oxide. It can be shown that the vertical electric field is lower for an SOI structure compared to a corresponding bulk-silicon device, resulting in a higher mobility. The relationship is as follows:

$$\mu_n(y) = \mu_{max} [E_c/E_{eff}(y)]^c \qquad \text{for } E_{eff}(y) > E_c \tag{2.3.1}$$

where μ_{max}, E_c, and c are fitting parameters depending on the gate oxidation process and the device properties, and

$$E_{eff}(y) = E_{s1}(y) - Q_{inv1}(y)/2\varepsilon_{si} \tag{2.3.2}$$

The vertical electric field below the gate is given by:

$$E_{s1}(y) = \{[\Phi_{s1}(y)-\Phi_{s2}(y)]/t_{si}\} + [qN_a t_{si}/2\varepsilon_{si}] \tag{2.3.3}$$

It has been shown that in the case of fully depleted devices operating with a low drain voltage ($V_{DS} \approx 0$), the expression of surface electric field (2.3.3) can be simplified [2,6]. If the back interface is depleted and close to inversion, $\Phi_{s1}-\Phi_{s2} \approx 0$, the surface electric field reduces to

$$E_{s1}(y) \approx [qN_a t_{si}/2\varepsilon_{si}] \tag{2.3.4}$$

For the case of the bulk-silicon device, t_{si} is the thickness of the bulk region. For the case of the SOI device, t_{si} is the thickness of the overlying silicon film. It can be seen

that because the thickness of the SOI film is very small compared to the bulk case, the vertical electric field is significantly less, and, hence, the mobility is greater. Figure 2.3.1 presents the electric field as a function of depth, x, in both a bulk-silicon device and a thin-film SOI device [2].

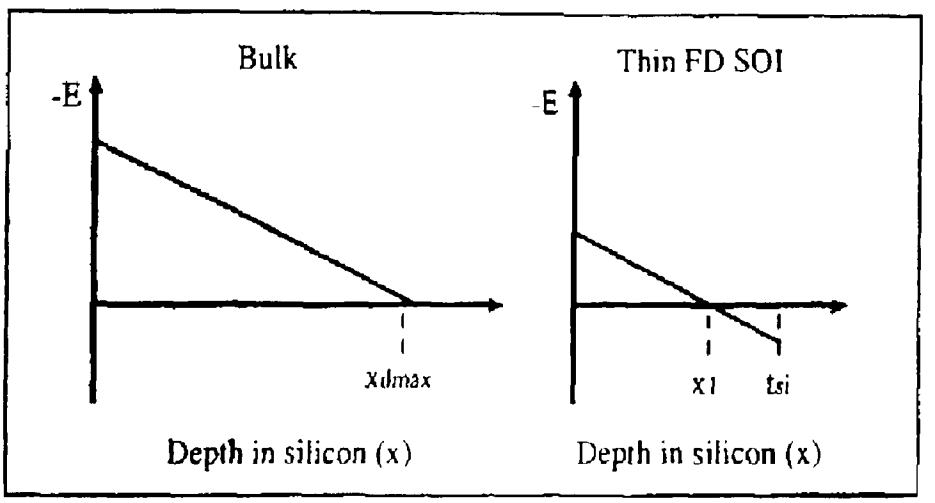

Figure 2.3.1: Electric field (x) in Silicon for a) a Bulk-Silicon Device, and b) a Thin-Film SOI Device.

2.3.2 Improved Subthreshold Slope

The inverse subthreshold slope or, in short, the subthreshold slope or subthreshold swing is defined as the inverse of the slope of the I_d (V_{gs}) curve in the subthreshold regime, as seen in Figure 2.3.2.

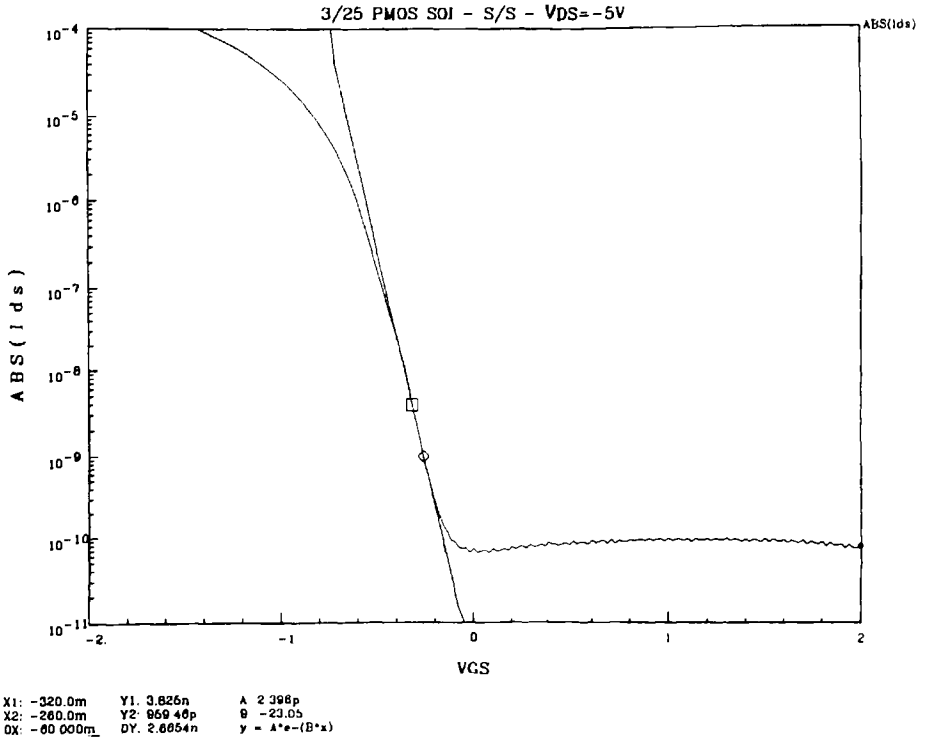

Figure 2.3.2: Subthreshold Swing of a PMOS SOI Device.

$$S = d(V_G)/\, d(\log I_D) \tag{2.3.5}$$

Using the relationship between gate voltage and charges both in the silicon and at the interfaces, and by neglecting the interface traps, a simplified relationship can be derived for subthreshold slope:

$$S = (kT/q) \ln [(10)\,(1 + \alpha)] \tag{2.3.6}$$

where $\alpha = C_b/C_{ox1}$. C_b and C_{ox1} are defined in the following paragraph [2].

The subthreshold swing is a measure which allows one to determine how well a device turns off, or how leaky a device is. As discussed previously, device parasitics have a significant effect on the speed of operation, and, therefore, it is imparitive to minimize the subthreshold swing. The SOI structure inherently possesses less parasitics

and, therefore, yields an improved subthreshold slope compared to that of bulk-silicon architectures. Comparing the two structures and breaking them down into the components which add parasitics gives better understanding of this result.

The bulk-silicon and SOI substrates are composed of parasitics, which can be represented by multipule capacitors in series. The bulk-silicon-equivalent capacitor network, as seen in Figure 2.3.3, is composed of two capacitors: an oxide capacitance, C_{ox1}, and, a diffusion capacitance, C_D.

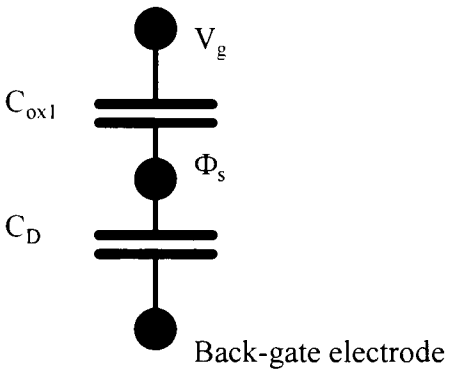

Figure 2.3.3: Bulk-Silicon-Equivalent Capacitor Network

(where $C_{ox1} = \varepsilon_{ox1}/t_{ox1}$, $C_D = \varepsilon_{si}/x_{dmax}$, and $\Phi_s = 2/3(\Phi_f)$)

At this point it is helpful to define a parameter, C_b, to be the capacitance between the inversion channel and the back-gate electrode. C_b, in the case of the bulk silicon structure is equal to C_D. Recalling Equation (2.3.6), the bulk-silicon subthreshold swing is equal to:

$$S = kT/q \ln [(10) (1 + C_d/C_{ox})] \qquad (2.3.7)$$

Looking at the SOI-equivalent capacitor network in Figure 2.3.4, we can see the presence of the additional underlying oxide capacitance, C_{ox2}, along with the capacitance of the silicon thin-film, C_{si}, and the top oxide capacitance, C_{ox1}.

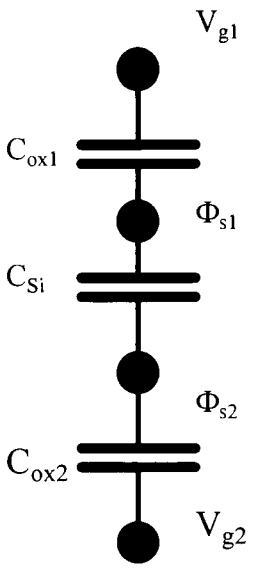

Figure 2.3.4: SOI-Equivalent Capacitor Network

(where $C_{ox1} = \varepsilon_{ox1}/t_{ox1}$, $C_{ox2} = \varepsilon_{ox2}/t_{ox2}$, $C_{si} = \varepsilon_{si}/t_{si}$, and $\Phi_s = 2/3\Phi_f$)

For the SOI-equivalent network, the two oxide capacitances can be taken in series. Because the thickness of the underlying oxide is much greater than the overlying gate oxide thickness, the series capacitance can be approximated as C_{ox2} [2]. Taking this result with Equation (2.3.6) yields:

$$S = kT/q \ln [(10) (1 + ((C_{Si} C_{ox2})/(C_{Si} + C_{ox2}))/C_{ox1})] \quad (2.3.8)$$

Being that $C_{ox2} << C_{ox1}$ and that $C_{ox2} << C_{si}$, the subthreshold slope can be approximated as:

$$S = kT/q \ln (10) \quad (2.3.9)$$

A mere comparison of Equations (2.3.7) and (2.3.9) shows that the inverse subthreshold slope of an SOI device will be lower than that of a bulk-silicon device having the same parameters. It can be seen that the bulk-silicon case will always be at least an order of (kT/q) ln (10 C_d/C_{ox}) higher than that of the SOI case. This translates to a corresponding theoretical lower limit of 60 mV/decade for an SOI structure, and something higher (depending upon capacitances) for bulk silicon [14]. With this inherent relationship, SOI offers a significant potential for performance gain.

Silicon-on-Insulator's driving force is the resulting lower subthreshold swing, improved mobility, greater ease of process, and an architecture which allows for smaller geometries. The three main driving factors have, and will continue to, bring forth advances which may make SOI a viable production technology.

Chapter 3 Types of Silicon-on-Insulator Materials

Many techniques have been developed for producing a film of single-crystal silicon on top of an insulating layer. Some of the techniques involve the epitaxial growth of silicon on either a silicon wafer covered with an insulator, or on a crystalline insulator (such as Silicon-on-Sappire, SOS) [2]. Other techniques are based on the crystallization of a thin silicon layer deposited on top of an insulator (laser recrystallization, electron-beam (e-beam) recrystallization, or zone-melting recrystallization) [2]. SOI material can also be produced using ion beam synthesis to isolate a thin silicon layer from the substrate (eg. SIMOX) [2]. Finally, SOI material can be obtained by thinning a silicon wafer which has been bonded to an insulator and a mechanically-supportive substrate (wafer bonding) [2]. Each approach has its advantages and disadvantages, and the type of application dictates which SOI material will be used. SIMOX, for instance, appears to be an ideal material for VLSI and radiation-hard applications; laser recrystallization is the best approach for 3D integration, while wafer bonding is more adept to bipolar and "Power" applications. This chapter reviews the techniques used to produce these materials, and compares their physical and electrical properties.

3.1 Silicon on Sapphire (SOS)

Silicon-on-sapphire (SOS) is the most mature of all SOI techniques. SOS was first conceived by Manasevit and Simpson in 1963 [15]. In 1975 RCA fabricated a 1k SRAM marking the first notable use of SOS [15]. SOS was used up to 1988, when a 64k CMOS SRAM, and a 4-bit, 1GHz Flash ADC were produced [15]. Until recently, SOS was the only SOI technology able to produce VLSI circuits. Due to its low mobility and carrier lifetime, and the introduction of newer and better materials, SOS has lost its attractiveness as a viable material. Historically, it is interesting to investigate its physical and electrical attributes to establish a "base line", or an understanding of how SOI technology has progressed.

The sapphire crystals are produced using either a flame fusion growth technique, Czochralski growth, or edge-defined, film-fed growth [16]. After chemical and mechanical polishing, the sapphire wafers receive a final hydrogen etching at 1150°C in an EPI reactor, and a silicon film is deposited using pyrolysis of silane. Due to thermal and lattice mismatch, defect density in the films is quite high, especially in a very thin film. The main defects found are aluminum autodoping from the sapphire substrate, stacking faults, and microtwins. Typical defect densities near the interface reach as high as 10^6 planar faults/cm and 10^9 line defects/cm^2 [17]. These account for low, undesirable values of resistivity, mobility, and lifetime near the interface.

3.2 Laser Recrystallization

Laser recrystallization is the recrystallization of deposited polysilicon on an insulating layer. This is accomplished by selective annealing, seeding, and raster-scanning a shaped laser beam (Figure 3.1) [2]. The vast majority of SOI experiments based on laser recrystallization have been carried out using Ar^+ lasers. The laser beam is focused on the sample by means of an achromatic lens into a circular or, more often, elliptical lens. The size of the molten zone and texture of the recrystallized silicon depend upon parameters such as laser power, laser intensity profile, substrate heating, and scanning speed. Typical recrystallization conditions of a 0.5-μm-thick LPCVD polysilicon film deposited on a 1-μm thermal oxide grown on a silicon wafer are: spot size of 50-150 μm, power of 10-15 watts, scanning speed of 5-50cm/sec, and substrate heating of 300-600°C [18].

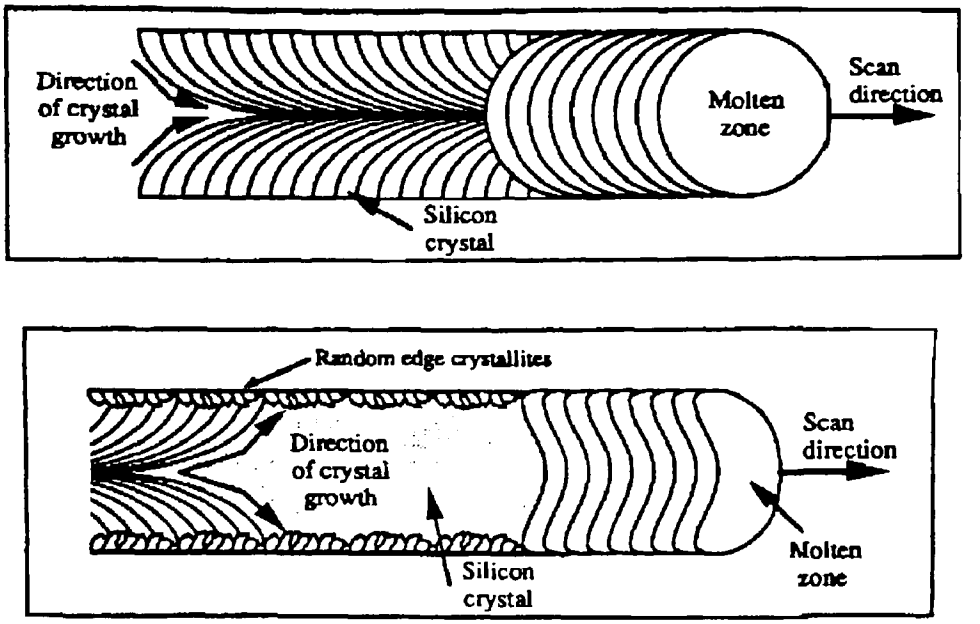

Figure 3.1: Laser Recrystallization Rastering and Beam Shape for a) circular and b) shaped laser spots.

The main obstacles associated with laser recrystallization are the ability to control silicon film thickness and to produce minimal crystal defects. Because of some surface tension and de-wetting effects, polysilicon films tend to "bead up" on SiO_2 upon melting. A surface thickness variation of at least 0.2 μm seems unavoidable unless planarization steps are performed. Grain boundaries and stacking faults are high, yet localized, found at the beam path edges. These problems result in poor mobilities and carrier lifetimes.

3.3 Electron-beam Recrystallization

The recrystallization of a polysilicon film on an insulator using an electron beam is in many ways very similar to, yet better than, the recrystallization using a laser. The use of an electron beam (e-beam) for recrystallization offers some potential advantages over a laser since the scanning of the electron beam can be controlled by electrostatic deflection, which is far more flexible than the galvanometric deflection mirrors used by

lasers. The absorption of the energy deposited by an electron beam is almost the same in most materials. This improves the recrystallization uniformity of silicon deposited over an uneven substrate [2].

A few e-beam recrystallization techniques are used. The most flexible technique entails the synthesis of a pseudo-linear source through rapid scanning of a focused beam (Figure 3.2) [2]. A continuous, linear molten zone can be created in the silicon film if the period of the scan is smaller than the thermal constant of the SOI system. This results in fewer grain boundaries, although still significant, when compared to the laser recrystallization method. Resultant stacking faults are of the same order of magnitude as compared to laser recrystallization.

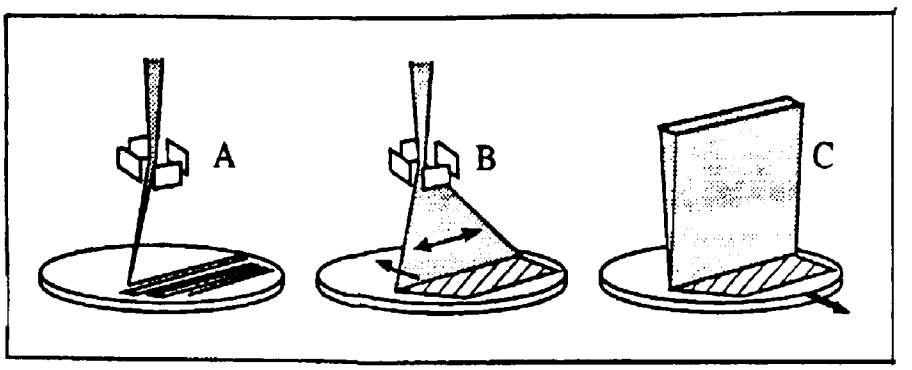

Figure 3.2: Electron-Beam Recrystallization Techniques. a) Serial Scanning, b) Parallel Scanning, fixed wafer, c) Parallel Scanning, moveable wafer.

3.4 Zone-melting Recrystallization (ZMR)

One of the main limitations of laser and e-beam recrystallization is the small molten zone produced by the focused beam. Because the molten zone is so small, a long processing time is required to recrystallize the entire wafer. Recrystallization of a polysilicon film on an insulator can also be performed using an incoherent light source. In this way, a narrow but long molten zone can be created on the wafer. A molten zone

length the size of an entire wafer diameter can easily be obtained. As a result, full recrystallization of a wafer can be performed in a single pass. This recrystallization technique is referred to as Zone-Melting Recrystallization (ZMR) because of the analogy between this method and the float-zone process used to produce silicon ingots.

The first ZMR method which successfully achieved large-area recrystallization makes use of a heated graphite strip which is scanned across the sample to be recrystallized. This setup is referred to as "graphite strip heater" (Figure 3.3) [19]. A resistively-heated graphite "susceptor" is used to bring the temperature of the sample to within a few hundred degrees below the melting point of silicon. Additional heating is locally produced at the surface of the wafer using a resistively-heated graphite strip, held a few millimeters above, and scanned across the wafer. A typical sample consists of a silicon wafer which has 1 to 2 microns of thermal oxide grown on it, followed by a 0.5 to 1-μm LPCVD polysilicon layer. A thin layer of silicon nitride is deposited over the polysilicon to protect the molten silicon from contaminants.

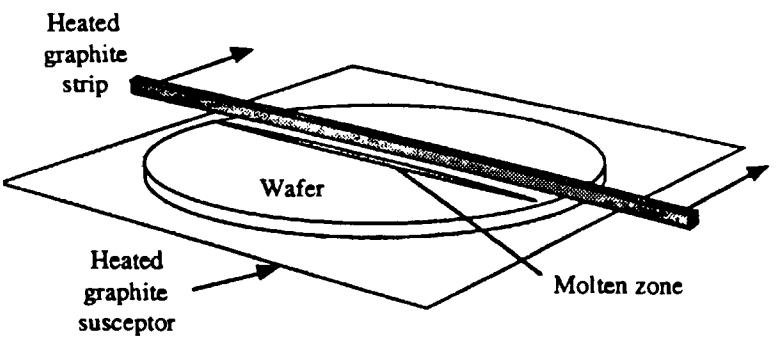

Figure 3.3: ZMR - Graphite Strip Heaters

Both the graphite susceptor and the strip can be replaced by lamps to achieve the ZMR of SOI wafers. A lamp system is composed of a bank of halogen lamps, used to heat the wafer from the back, and a top halogen or mercury lamp, focused on the sample by means of an elliptical reflector (Figure 3.4) [20].

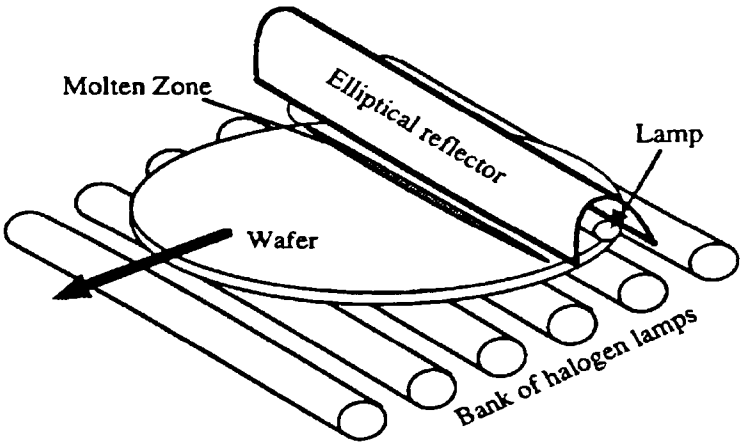

Figure 3.4: Halogen Lamp Heaters

Both of the ZMR recrystallization techniques yield subgrain boundaries and dislocations in medium densities when compared to other recrystallization techniques. This yields a technology which exhibits better mobilities and carrier lifetimes. Thickness uniformity is still a problem and limits the applications of this material.

3.5 SIMOX

One of the most popular approaches currently used to provide SOI material for commercial CMOS fabrication is Separation by IMplanted OXygen (SIMOX). The principle behind SIMOX material formation is simple. It involves the formation of a buried SiO_2 layer by implantation of oxygen atoms beneath the surface of a silicon wafer (Figure 3.5) [2]. Processing conditions must be such that a single-crystal overlayer of silicon is maintained above the buried oxide. Ion implantation is used to synthesize a new material, namely SiO_2. Two atoms of oxygen must be implanted for every silicon atom to the depth at which the silicon dioxide is to be formed. This requires a high dose which is approximately 200-500 times the heaviest doses commonly used in

microelectronics. After the implantation, a high-temperature anneal must be performed to repair the damage to the crystalline silicon overlayer and to electrically activate the oxygen ions. SIMOX provides ultrathin silicon films on the order of 800 Å to 5000 Å thick. The average thickness uniformity is approximately +/- 7%, which is adequate for CMOS designs [2]. SIMOX is less flexible regarding the buried oxide layer thickness. This limitation makes low-capacitance designs difficult. The silicon film is also limited by dislocation densities of approximately $10^4/cm^2$, thereby preventing use of SIMOX for bipolar applications. In comparison to all previously-mentioned technologies, SIMOX offers superior mobilities and thin-film thickness control. The minority carrier lifetimes resulting from SIMOX are greater than the previously mentioned technologies, with the exception of ZMR.

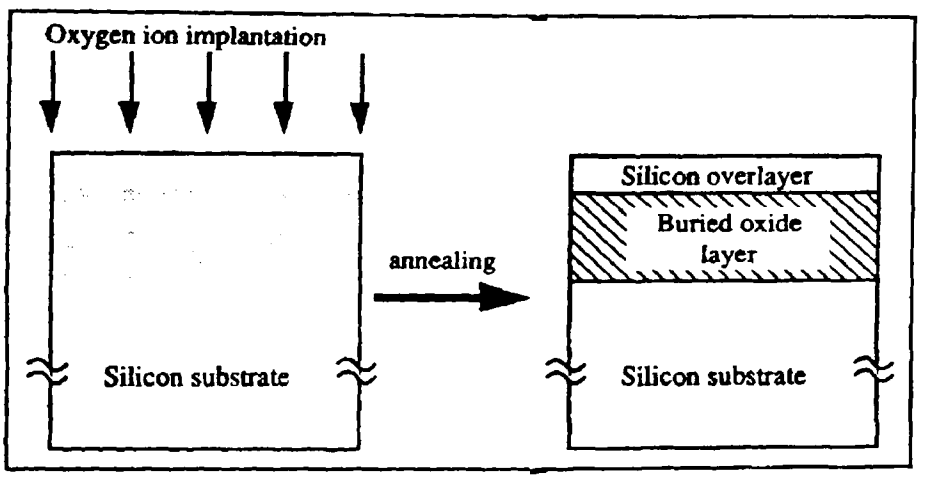

Figure 3.5: SIMOX

3.6 Bonding and Etchback

Another very promising SOI technology is the bonded-wafer technique. This technique involves the thermally-assisted bonding of two oxidized wafers and the controlled thinning of one wafer down to the desired silicon thickness by grinding, polishing, and chemical etching (Figure 3.6) [21]. The other wafer serves as the

mechanicallysupportive substrate. This technique offers wide flexibility in choosing the silicon and the underlying insulating films. The bonded-wafer technique is also the most cost-effective SOI fabrication process, with far superior physical and electrical attributes. The main drawback of the bonded technique is the inability to produce ultra-thin silicon films (< 1 micron). While 1 micron is adequate for bipolar applications, submicron CMOS requires film thicknesses of approximately 0.1 microns with thickness uniformities of +/- 5% [2]. The bonded-wafer technique is currently being developed, including the work herein, and shows promise of becoming a viable production process. The primary reason bonded-wafer technology offers promise is that the resulting silicon film is comparable to bulk silicon both electrically and physically, with high mobilities and carrier lifetimes, and low defect densities. With advances in film thickness control, the bonded-wafer technology could easily replace conventional bulk-silicon architectures.

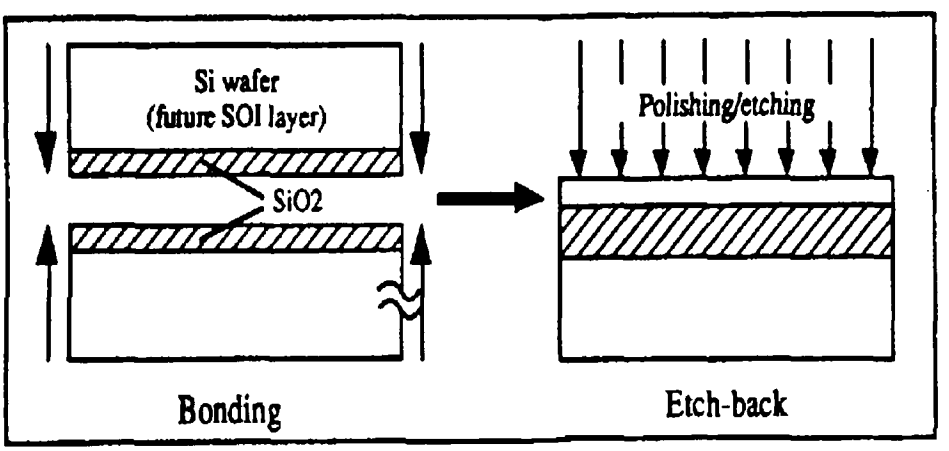

Figure 3.6: Bonded and Etched-Back Process

3.7 Physical and Electrical Comparison Summary of SOI Materials

Summarized in Table 3.1 are the types and contrations of crystal defects found in various SOI materials discussed throught Chapter 3. Table 3.2 compares the physical and electrical properties of the SOI materials from Table 3.1, benchmarked against a bulk-silicon reference.

Types of Defects

Material	Type of Defect	Concentration
SOS	Microtwins, Stacking Faults	High
Laser	Grain Boundaries, Stacking Faults	High, localized
e-beam	Grain Boundaries, Stacking Faults	High
ZMR	Subgrain Boundaries, Dislocations	Medium
SIMOX	Dislocations	Low
Bonding/Etchback	Dislocations	Low

Table 3.1: Types of crystal defects present in different SOI materials [2].

Types of Defects

Material	Defect Density	Thin Si Film Thk. Control	Minority Carrier Lifetime	Channel Mobility
SOS	--	0	--	--
Laser	0	-	0	0
e-beam	0	-	0	0
ZMR	+	-	+	+
SIMOX	+	+	0/+	+
Bonding/Etchback	++	--	++	++
Bulk Silicon	++	N/A	++	++

Table 3.2: Comparison of some physical and electrical properties of different SOI materials (bulk Si properties are indicated as a scale reference) [2].

++= very good, += good, 0= average, -= poor, --= very poor

Chapter 4 Applications of SOI Materials

CMOS remains the most obvious field of application for SOI: SOI's ease of processing and full dielectric isolation advantages have sparked much research activity. Structures such as gated diodes, lateral bipolar and bipolar-MOS devices, vertical bipolar transistors with back gate-induced collectors, high-voltage lateral devices, and double-gate MOS devices have been proposed [22,23]. Each application's physical and electrical characteristics determine which SOI technology is necessary. Thick SOI films, such as those produced by the bonding and etchback technique, are suitable for "Power", high voltage, and bipolar applications [22,23]. Radiation-hard and VLSI CMOS devices require properties which SIMOX offers. Laser, electron-beam, and large-grain techniques for recrystallization of polysilicon techniques are required for three-dimensional (3-D) integration [24]. SOI technology is also able to implement not only conventional devices adapted from bulk silicon, but also devices which are difficult or impossible to fabricate in bulk silicon. SOI technology opens the door to new possibilities in device design.

4.1 Applications of Laser, E-Beam, and Large-Grain Recrystallization of Polysilicon

The most attractive use of the recrystallization of polysilicon by laser or e-beam, is 3-D integration. Laser and e-beam recrystallization are used preferentially to other SOI techniques such as ZMR because the beam heats only the top polysilicon layer. Also, the dwell time is short enough to avoid degradation of devices which reside below the layer being recrystallized. Three-dimensional circuits are fabricated by stacking several device layers on top of one another. The first layer is usually fabricated in a bulk-silicon wafer (or SIMOX may be used) using classical processing techniques. An insulating layer of silicon dioxide is then deposited, followed by a layer of LPCVD polysilicon. Laser or e-beam recrystallization is then used to melt and recrystallize the polysilicon layer into

device-worthy silicon. Figure 4.1 presents an example of a CMOS stacked inverter, where the n-channel device is in the bulk-silicon substrate [2]. 3-D integration offers a significant increase in packing density by adding on an entire dimension. Figure 4.2, a parallel and serial data processing comparison, and Figure 4.3, a 3-D character recognition chip, depict how 3-D integration can be used to greatly compress area and increase speed of operation [2].

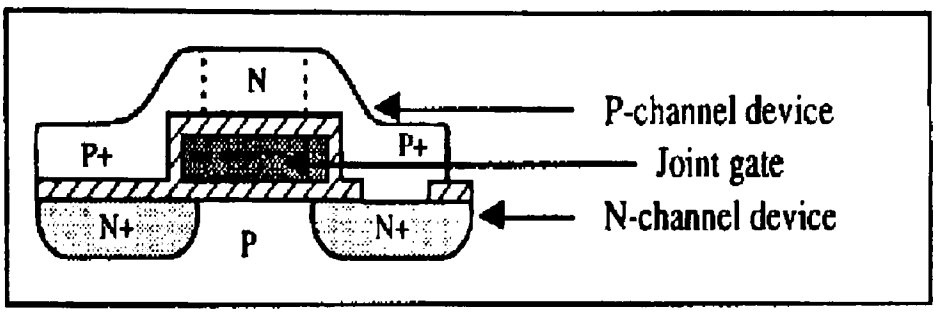

Figure 4.1: CMOS Stacked Inverter

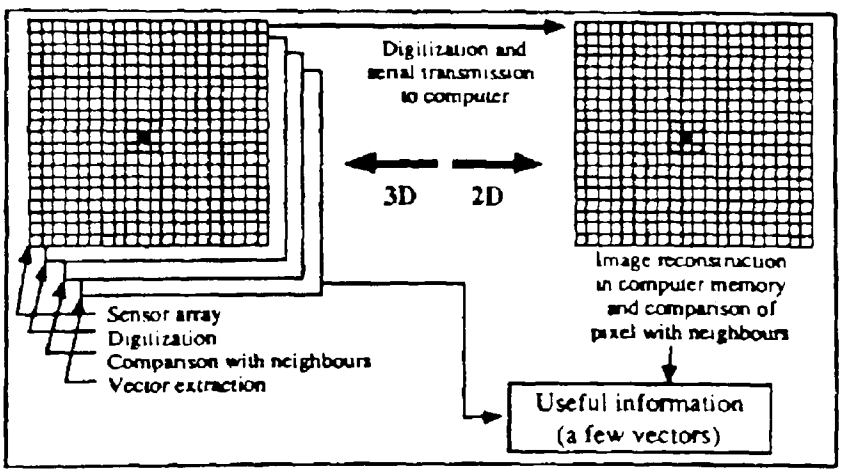

Figure 4.2: Parallel and Serial Data Process Comparison

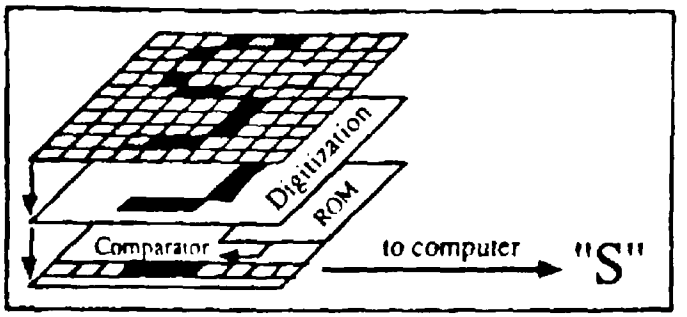

Figure 4.3: 3-D Character Recognition

4.2 SIMOX Applications

Two of the most notable applications for the SIMOX SOI technology are radiation-hard devices and VLSI CMOS devices. SIMOX is key to VLSI CMOS applications because of its ability to produce the ultra-thin silicon layers required to avoid short-channel effects in submicron devices. Radiation-hard devices rely on SIMOX for the same ultra-thin film.

One of the major market niches where SIMOX SOI devices are currently being used is the aerospace and military market, because of the devices' high resistance to radiation effects. The effect of radiation on an electronic device depends upon the type of radiation to which the devices are exposed. MOS devices are very sensitive to exposure to single-event upset (SEU), gamma-dot upset, and total-dose exposure. SEU is caused by the penetration of an energetic particle, such as an alpha particle or a cosmic ray, into the substrate. When such a particle penetrates a reverse-biased junction of a bulk-silicon device, a track of ionized silicon is created in the junction depletion layer and the bulk silicon underneath it. The presence of this track temporarily collapses the depletion layer and distorts the electric field in the vicinity of the track. The distortion of the depletion region is referred to as a funnel (Figure 4.4) [25]. The funnel produces a large electric field such that the electron-hole pairs are separated. In a bulk-silicon device, the

electrons move up the funnel into the depletion layer, while the holes move downward and create a substrate current. The electrons result in a large increase in charge, which can affect the logical state of the node. In an SOI device as well, the impinging particle ionizes the silicon along the track. However, because of the buried insulating layer between the active silicon film and the substrate, none of the charges generated within the substrate can be collected by the junctions of the SOI device. The only electrons which can be collected are those produced within the thin silicon film. This smaller collection of charge is much less likely to cause a logic upset. SIMOX technology is indispensable in producing radiation-hard devices because it is imperative to have a very thin film, and because CMOS devices are the most prone to radiation effects.

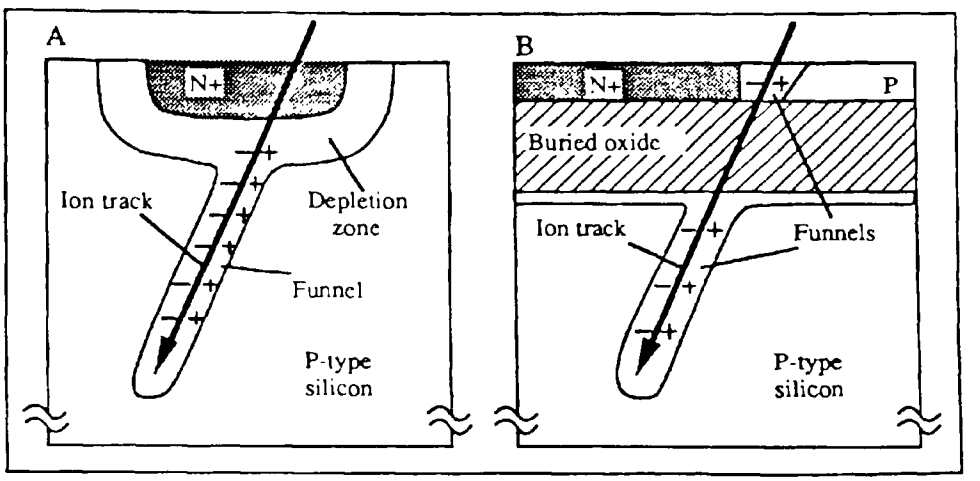

Figure 4.4: Disturbance of Depletion Layer by a Charged Particle

4.3 Wafer-Bonding and Etch-Back Technology Applications

Wafer-bonded SOI technology shows the greatest promise of replacing bulk-silicon architectures, provided that its one limitation, namely thin-film thickness control, is resolved. Currently, wafer-bonding technology is being used for "Power", high-voltage, and bipolar devices, as well as for devices which require mobilities, carrier

lifetimes, and defect densities comparable to bulk silicon. Figure 4.5 shows a high-voltage SOI MOSFET [26]. Breakdown voltages of 90 volts are obtained for an active silicon thickness of 4000 Å and a gate thickness of 1000 Å. The previously-mentioned flexibility of the bonded etchback process allows for the silicon-on-oxide-on-silicon-on-oxide structure as seen in Figure 4.5. Figure 4.6 shows a vertical bipolar transistor with a gate-induced buried collector [27]. The nature of bipolar devices requires very low defect densities, and, thus the bonded wafer technique is the only viable SOI technology. Currently, work is being done, including the work herein, to control silicon films to very small thicknesses. Once this has been accomplished, bipolar and CMOS devices can be produced on a single SOI substrate, with the active silicon of equal quality to bulk silicon. This has enormous potential for device applications, especially because the bonded-wafer technique is the most cost-effective. Future applications may include digital signal processors and BiCMOS devices. This could lead to the obsolescence of conventional bulk-silicon architectures.

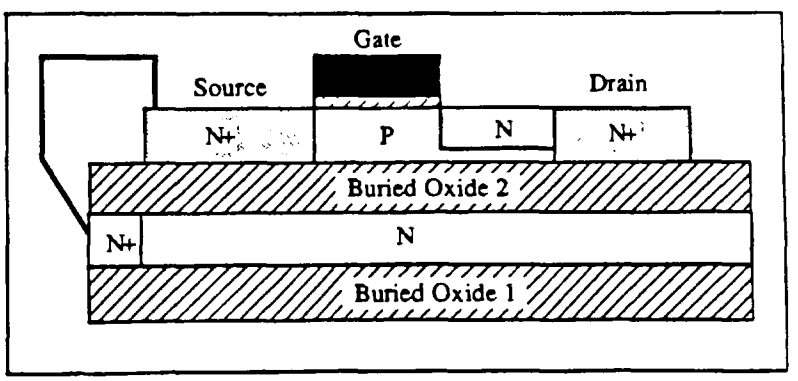

Figure 4.5: High-Voltage SOI MOSFET

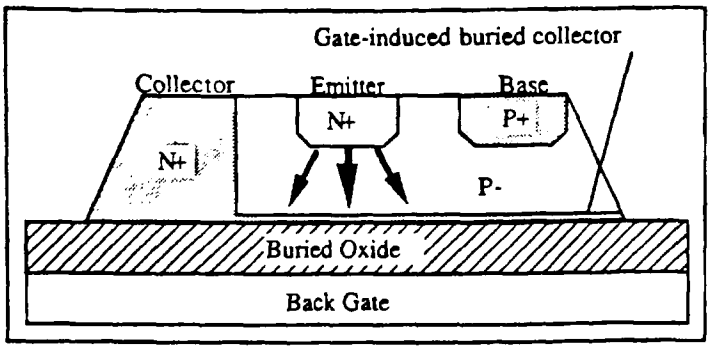

Figure 4.6: Vertical Bipolar Transistor with Gate-Induced Burried Collector

Chapter 5: Key Issues in Silicon-On-Insulator Technology

The foremost consideration or limitation to using SOI technology as a viable production process is cost of manufacturing. Considering that a device must be produced which exhibits, at a minimum, comparable device characteristics (speed, gain, leakage) to that of bulk-silicon devices, and that this must be done at the smallest cost, the bonded, etched-back (B-E) SOI technology shows the greatest promise. Unlike other SOI technologies, the B-E process yields devices which have high mobilities, low leakages, and high carrier lifetimes, with a process which is less expensive. This process shows great potential for increasing the device performance of VLSI CMOS devices, providing that a few key material-related and device-related issues are resolved. Among the key issues which need to be resolved are silicon thin-film uniformity, defect density, and back-channel effects.

The silicon thin-film uniformity of the B-E process presents the largest challenge, as it is the key factor which limits CMOS devices from yielding well. With this issue resolved, devices superior to those realized in bulk silicon can be fabricated. The remainder of this paper investigates the results of a technique whereby a thin, uniform film of silicon was produced on an insulating layer using a bonded and etched-back process. It will be shown that, with this key issue resolved, devices superior to their bulk-silicon counterparts can be fabricated. The advantages of this SOI technology, which positively impact both process and device characteristics, will be discussed and compared to those of bulk silicon. In addition, the relationship of these characteristics will be defined, measured, and related to real experimental data.

Chapter 6: Experimental

The purpose of this endeavor, as previously described, was to investigate the impact on device performance exhibited by a new bonded and etched-back process, having a uniform, thin-film of silicon. To do this, "test" devices had to be designed and fabricated to extract device characteristics. The work required to yield the results and conclusions contained within can be segregated into five areas: substrate preparation, device design, process design, device fabrication, and finally, device parameter extraction.

6.1 Substrate Preparation

The B-E SOI substrate preparation is the key to yielding high-speed, low leakage CMOS devices. For comparison or benchmarking, two additional substrate-types were prepared and processed in parallel with the B-E SOI wafers, the most important of which is the bulk silicon. CMOS device parameters are well-defined for Rochester Institute of Technology's standard CMOS process. The parameters extracted from the bulk-silicon devices can, therefore, be compared to both the B-E SOI devices as well as to standard RIT CMOS devices. The other substrate included is polysilicon. The reason for this inclusion was to benchmark the B-E process to a very similar one developed at RIT by Louigi Ternullo [28]. Being that many of the changes to the RIT CMOS process were included in Ternullo's procedure, comparing the results of a substrate of his design, processed through the current B-E process, has been very insightful.

6.1.1 Bonded and Etched-Back SOI Substrate Preparation

Work was done at IBM, East Fishkill, NY, to produce a high-quality, uniformly-thick, thin-film of device-quality silicon on silicon dioxide. Figure 6.1 depicts the stages of the B-E SOI substrate formation [21]. First, an N-type wafer (substrate 1) was subjected to an oxygen atmosphere at high temperature to grow a thermal oxide. Second,

a thin layer of SiGe was deposited on a separate P-type wafer (substrate 2) by high-temperature epitaxy. Following this, 2000 Å of undoped (100) silicon was eptaxially grown, after which a thermal oxide was grown. Substrate 2 was inverted and placed on substrate 1 after a chemical treatment. The wafers were then exposed to a high temperature to permanently bond them together. Next, the top of the new substrate was polished mechanically and chemically down to the SiGe layer. The SiGe layer was removed, leaving the 2000 Å of epitaxially-grown (100) silicon.

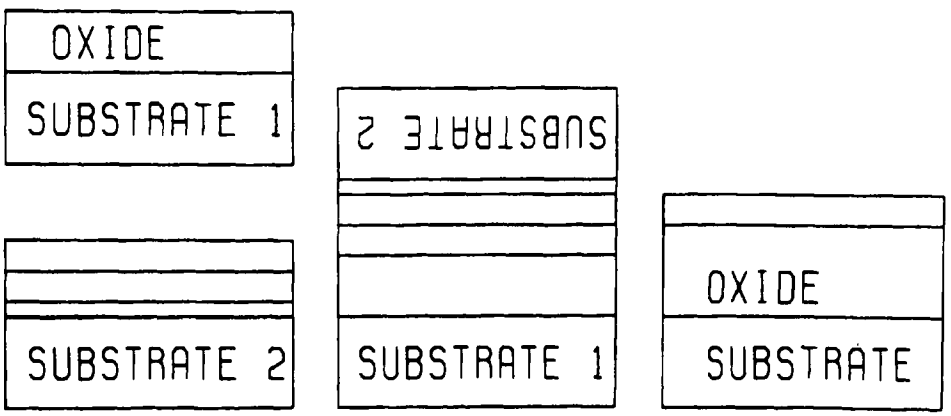

Figure 6.1: Bonded and Etched-Back SOI Substrate Formation

6.1.2 Polysilicon Substrate Preparation

The polysilicon substrates were prepared by first growing 3000 Å of thermal oxide on a P-type wafer and then depositing 2000 Å of LPCVD polysilicon. This substrate preparation matches that of Louigi Ternullo's, and thus makes it suitable for device comparison following fabrication [28].

The bulk-silicon devices were also chosen to be P-type because of availability.

6.2 Device Design

The first step in the process was to design devices and test structures which would yield the required parameters for evaluation and take advantage of the SOI technology being used. Previous work performed by Louigi Ternullo and Robert Pearson supplied a design which was adequate for this process [28,29]. Ternullo's and Pearson's work was in polysilicon thin-film transistors, which happen to have the same substrate structure, namely silicon (polysilicon in this case) on silicon dioxide. Their projects are suitable for 3-D integration because a polysilicon recrystallization process is used to produce the substrate. However, their designs lacked a ring oscillator which would show a direct speed correlation between the B-E SOI structure and the bulk-silicon structure. Due to a heavy backlog for making stepper radicals on RIT's MEBIS system, which would have greatly delayed the project, it was decided that Ternullo's and Pearson's design was best suitable.

The physical design layout was performed on an Apollo workstation using Mentor Graphics' Chipgraph. Six layers were defined and used to realize the design. The levels in order of processing are as follows: MESA for transistor isolation; POLY for the gate electrode; P^+ and N^+ for the PMOS and NMOS source and drain implants, respectively; CC for the contact cuts; and METAL for the metal interconnects. MOSIS CMOS design rules were chosen with a lambda value of 3 μm. This corresponds to contact cuts of 6 μm X 6 μm (the smallest feature size) and a minimum metal line width of 12 μm.

NMOS and PMOS transistors were designed with virtually all possible gate lengths and widths ranging from 2 to 50 μm. Figure 6.1 shows the schematic layout of an NMOS transistor with all layers labeled [28]. The figure depicts how the MESA mask isolates each transistor, defining a 300 μm X 300 μm silicon island. The metal bond pads are each 100 μm X 100μm, separated by 100 μm minimum on each side. Each transistor was designed as a four-terminal device with connections to the source, drain, gate, and substrate. Future designs should call for a back-side contact, as will be discussed later.

The substrate contact is a Schottky contact, unlike the source, drain, and gate, which are ohmic. A direct contact to the substrate was made with the assumption that the Schottky diode voltage drop would be negligible compared to the substrate-drain diode voltage drop [28].

In addition to the transistors designed, other test structures were included to assist in device and process characterization. Among these were Van der Pauw structures to measure sheet resistance, Kelvin contact resistance structures, capacitors for CV analysis, and diodes to test for source/drain-to-substrate leakage. Other structures were included for lithographic considerations. These include line-resolution and square-resolution patterns ranging from 1.0 μm to 10.0 μm, designed to test the following: the steppers' ability to resolve an image, verniers for recording inter-level alignments, and stepper alignment marks for in-process alignment on the stepper. See L. Ternullo, Jr. and R. Pearson for the complete test chip design [28,29].

After the layout was completed, the file was stored in Cal Tech Intermediate Format, or a CIF file. The CIF file was then transferred to a CATS system where the layout was fractured into its individual layers composed of rectangles, and saved to magnetic tape with other information required to generate the stepper radicals. This set of instructions was carried out on RIT's MEBIS system, yielding two redicles: one containing levels 1 - 4, and the second containing levels 5 and 6.

6.3 Process Design

The process design was carried out using TMAs' SUPREM III and SUPREM IV simulation tools. The base process was borrowed from RIT's CMOS process. RIT's CMOS process has been developed over 3 years by Dr. Lynn Fuller and his Mircoelectronic Engineering graduate and undergraduate students, yielding good prediction of equipment response. Changes were made in the simulation to yield the appropriate film thicknesses, junction depths, and sheet resistances, which were then

carried into the actual process. The resulting parameters for the entire process can be found in detail in Appendix A. Important specifics of the significant process steps are given in the sections that follow.

6.4 Device Fabrication

6.4.1 Gate Oxide

RIT's horizontal furnace tube #12 underwent a TCA clean for 15 minutes at 900°C prior to gate oxide growth. TCA, at a temperature of 25°C, was delivered into the tube by bubbling 190 sccm of N_2 through the TCA. Next, 0.5 Slm of O_2 and 4.5 Slm of N_2 was flown and the wafers were pushed in at 12 in./min. The temperature was ramped from 900°C to 1100°C at a rate of 13.3°C per minute. The soak time was 13 minutes with 4.0 Slm of O_2 at 1100°C. The furnace temperature was ramped down from 1100°C to 900°C at 7°C per minute with 4.5 Slm of N_2 flowing. The resulting gate oxide thickness was 732 +/- 12 Å.

6.4.2 Gate Electrode Formation

The wafers were immediately placed into RIT's LPCVD furnace for polysilicon gate deposition following gate oxide growth. The furnace was previously characterized to deposit 66.7 Å/min. at 608°C, 610°C, and 611°C for load, center, and source (depletion reaction), respectively, flowing 90 sccm of SiH_4 with a process pressure of 325 mtorr. Deposition was carried out for 60 minutes, yielding a thickness of 5687 +/- 23 Å.

The polysilicon gate was doped using Emulsatone N-250 spin-on dopant (arsenic in methyl and ethyl alcohol). The N-250 was spun on at 3000 rpms for 10 seconds and baked at 185°C for 15 minutes. The dopant was diffused by placing the wafers into RIT's vertical furnace, tube #13, at 900°C for 20 minutes, while flowing 0.5 Slm O_2 and 4.5 Slm N_2. After removing the wafers from the furnace, they were deglazed in buffered oxide etch (BOE). The resulting sheet resistances for the polysilicon gates were 52.4

Ω/sq. for the B-E substrates, 72.0 Ω/sq. for the single-crystal substrates, and 52.8 Ω/sq. for the polysilicon substrates.

The patterning of the gate was a very crucial step. From previous experience, large areas of exposed positive resist would not be removed completely after develop, causing gate width and length dimensions to become larger. This was solved by including a "double-puddle" routine in the develop program, whereby the developer is dispensed on a static chuck and spun off after a given soak time [28]. Patterning was carried out using RIT's RIE, flowing a 30:3 mixture of SF_6 to O_2, with a process pressure of 75 mtorr and 75 watts of power. This gave an etch rate of 3000Å/min., requiring a 1.75-minute etch. All geometries down to 2 μm were resolved.

6.4.3 Source/Drain Formation

The wafers were patterned for a P^+ self-aligned source/drain implant. The implants were performed using B^{11} at an energy of 35 keV and a dose of $1x10^{15}$ ions/cm^2, determined using SUPREM 3 (Appendix B). The energy was chosen to place the peak of the implant in the vertical center of the SOI film thickness (1000 Å deep). A beam current of approximately 6 μA was the maximum attainable current at 35 keV. This required approximately 40 minutes for each wafer to reach the desired implant dose. Implanting the substrates such a large dose caused the resist to burn into the wafer. This caused difficulty in removing the resist by ashing. Finally, the resist was removed using a heated piranha bath for 30 minutes.

After the resist was removed, the N^+ source/drain was patterned. The implants were performed using P^{31} at an energy of 55 keV and a dose of $1x10^{15}$ ions/cm^2, determined using SUPREM 3 (Appendix B). The energy was increased from the P+ implant because phosphorous is more massive, and thus requires more energy to place the peak in the center of the SOI film.

After implant anneal, which was carried out at 900°C for 35 minutes in 5 Slm of O_2 (this grows approx. 200 Å of oxide over the poly gate), the N^+ sheet resistance was measured at 124 Ω/sq. and the P^+ sheet resistance was measured at 161 Ω/sq.

6.4.4 Passivation

LTO deposition was performed, flowing 12% O_2 and 20% SiH_4 (24 sccm and 40 sccm, respectively) at 400°C with a process pressure of 345 mtorr. Based upon previous experience, 10 dummy wafers were placed in the load end of the boat to act as baffles for promoting thickness uniformity across the run. Additionally, the process gasses were ramped up slowly, O_2 being first, to prevent any chance of polysilicon deposition. This was also done to prevent pressure spikes over 400 mtorr which would cause the furnace process controller to abort. The results were not ideal, yielding thicknesses ranging from 1165Å to 1864Å (Average was 1675Å) after an 80-minute deposition. Although a thicker, more uniform film was desired, the minimum thickness was decided to provide an adaquate inter-layer dielectric.

Following the deposition, LTO densification was performed at 900°C for 10 minutes in 5 Slm of dry O_2. The densification was performed to decrease the etch rate of the LTO, making it more comparable to that of thermally-grown oxide. Even following this step, the LTO etch rate, at 2400 Å/min., was approximately two times faster than that of the underlying oxide.

6.4.5 Contact Cut and Metallization

The wafers were patterned for contact and etched in BOE for 3.5 minutes. At this point, the contacts appeared to be cut clear to the source/drain and poly gate surfaces. Due to the increased LTO etch rate, the contacts appeared to look larger than defined by the photoresist. Being that a 3.5-minute etch was performed with an LTO thickness of 1600 Å and an LTO etch rate of 2400 Å/min., approximately 1 micron of lateral etch was

observed on the top LTO layer. The wafers were then stripped of photoresist following a careful inspection of each wafer's contact cuts.

Metallization was performed using an evaporator because the sputterer was not operational at the time of deposition. A base pressure of $1x10^{-5}$ torr was observed before passing current through a tungsten filament basket containing 1 gram of aluminum/1%-silicon. This yielded a film thickness of 4000 Å.

The wafers were sintered for 30 minutes in 5 Slm of forming gas at 450°C. After this, the wafers were patterned and etched in wet Al etch for 3 minutes. The wafers were ready for testing after resist strip.

6.4.6 Device Fabrication Problems

A major problem was discovered when testing the devices for the first time. Simply put, the devices did not work. In testing numerous structures designed to test the individual components of the device, it was determined that the devices did not work because there was a very high contact resistance present.

The first course of action taken was to place a high voltage onto the contact to see if any existing, underlying oxide, could be broken down. This was done successfully and indicated that the contact cut step was not effective.

The second course of action was to strip off the metal on one of the device wafers and inspect the contacts more closely. Upon measuring a number of contacts with a Nanometrics/Nanospec film thickness measurement system, it was discovered that approximately 200 Å of oxide still remained. This oxide corresponded to the thickness grown during implant anneal. It was decided to repattern the wafers with the contact cut mask and re-etch the wafers. Repatterning and re-etching proved to be ineffective; the remaining 200 Å of oxide could not be removed in the BOE.

It was speculated that there might be something on top of the thermal oxide, prohibiting the BOE to etch the oxide. Upon consultation of Dr. Richard Lane and Dr.

Santosh Kurinec of RIT's Microelectronic Engineering staff, two rework processes were proposed. The first comes from speculation of what the layer or barrier might be. It was thought that there may have been organic contamination on the wafers prior to LTO deposition. This could have resulted from a contaminated LPCVD tube, or from residual photoresist. The residual photoresist could have been left over from the implant steps, having not been successfully removed after hot piranha strip or RCA clean. The second theory was that there might be a chance, however, slight, that a thin layer of polysilicon was deposited while ramping up gasses during LTO deposition. This theory was weak because SiH_4 does not disassociate to form polysilicon at 400°C.

Both rework processes were tried and successfully resulted working devices. Appendix C presents the detailed steps contained within each rework process. The first rework process consisted of stripping the metal off, cleaning, and growing a thin oxide of approximately 300 400 Å. After this was done, the contacts were repatterned; Al was sputtered and patterned, and the devices were retested. The idea behind this process was that growing an oxide would consume any barrier or layer on top of the implant anneal oxide. This process worked well, was simple, and yielded working devices.

The second rework process also resulted in working devices as well, but, due to the plasma chemistry that was used, the gate electrode was attacked and etched. More work needed to be done to optimize the control of this process. Due to the success and ease of the first process, it was chosen and the second was discarded.

6.5 Device Parameter Extraction

After working devices were fabricated, parameters were extracted. There are a number of techniques used to measure various parameters. These techniques can be defined in slightly different ways, resulting in values which differ. To avoid any confusion as to how a parameter was extracted, each parameter will be defined and the procedure to extract it will be discussed. The parameters measured were effective

mobility, threshold voltage, subthreshold swing, and off-state leakage current. A corresponding maximum interface trap density (D_{it}) and interface trap capacitance (C_{it}) were calculated as well.

6.5.1 Effective Mobility Extraction

The effective mobility was extracted from the I_{DS} versus V_{GS} curves for both the linear region and the saturation region, where the device actually operates [6]. A standard, simplified relationship for mobility, taking into account the effective channel length, was used and is given by:

$$\mu_{lin,eff.} = \Delta Ids/\Delta Vgs\ (L_{eff}/W)\ (1/C'_{ox})\ (1/V_{DS}) \qquad (6.5.1)$$

where $C'_{ox} = \varepsilon_{ox} / t_{ox}$ and $L_{eff} = L - 2X_j$

$$\mu_{sat,eff.} = \Delta SQRT(I_{DS})\ /\Delta Vgs\ (L_{eff}/W)\ (1/C'_{ox}) \qquad (6.5.2)$$

where $C'_{ox} = \varepsilon_{ox} / t_{ox}$ and $L_{eff} = L \quad 2X_j$

As seen in Equation (6.5.1), the effective mobility in the linear region is dependent upon V_{DS}. Rather than fix V_{DS}, it was decided to trace the I_{DS} versus V_{GS} curves for ranges of V_{DS} values to determine where the device no longer depended upon the drain-to-source voltage (onset of saturation). Figure 6.5.1 is a typical plot showing the slope of the curve by connecting a line between two points in the linear region of the I_{DS} versus V_{GS} curve.

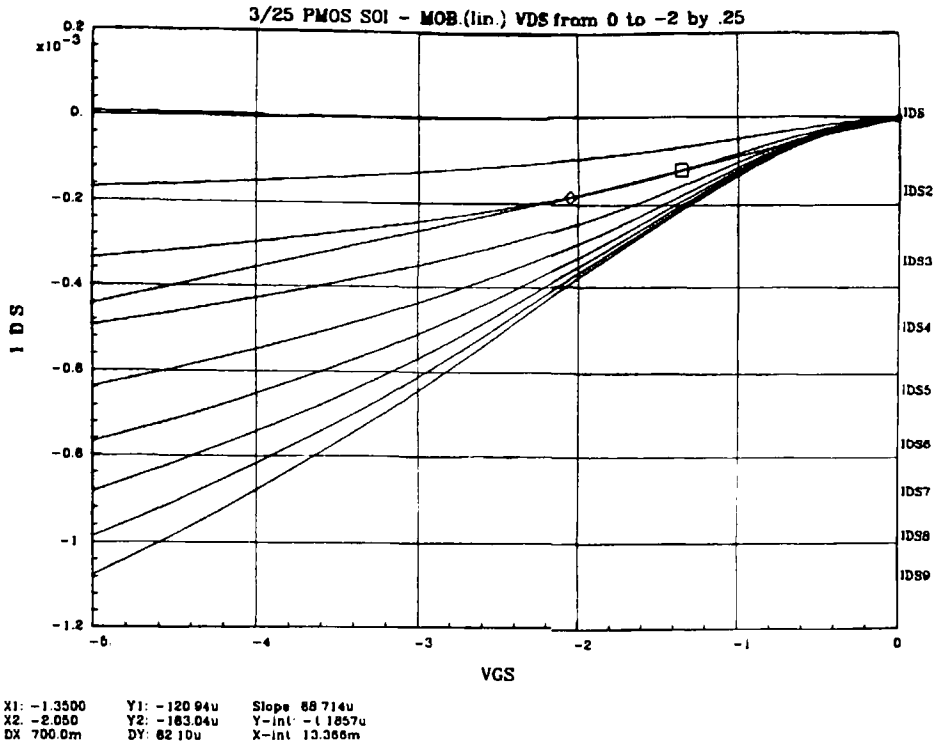

Figure 6.5.1: I_{DS} versus V_{GS} Curve - Mobility in Linear Region

As seen in equation (6.5.2), the effective mobility in the saturation region is not dependent upon V_{DS}. In this case, a drain-to-source voltage was chosen such that the device would be in saturation and the square root of I_{DS} was plotted versus V_{GS}. As before, the slope of the line was taken, yielding a tyical plot as seen in Figure 6.5.2.

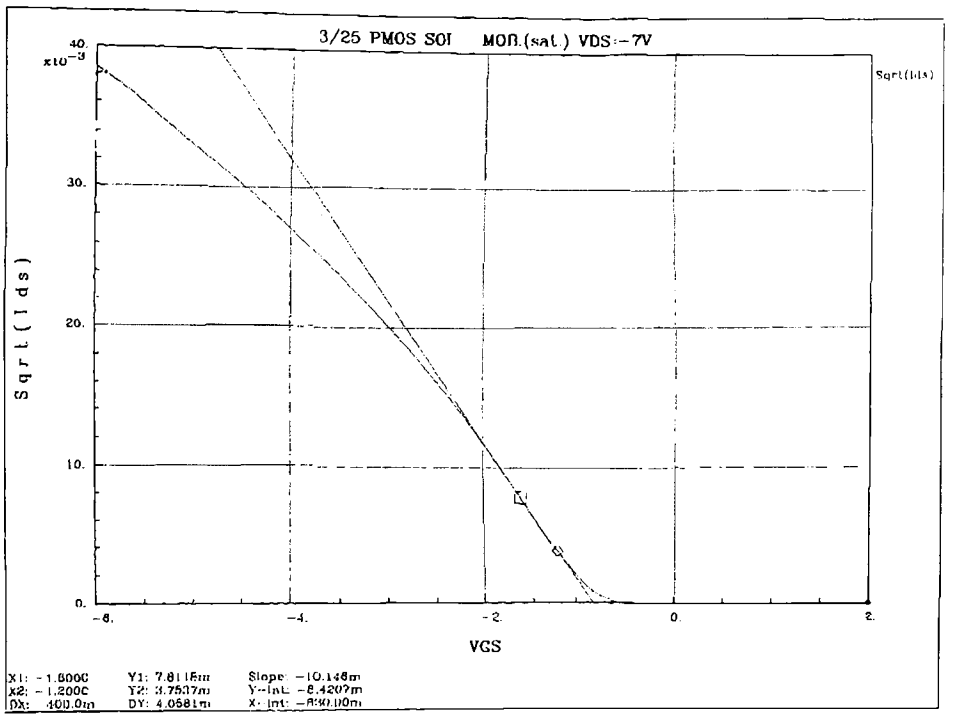

Figure 6.5.2: $(I_{DS})^{.5}$ versus V_{GS} Curve - Mobility in Saturated Region

After the slopes were extracted in each case, the effective mobilities were calculated from Equations (6.5.1) and (6.5.2). The effective channel length had to be considered because of the combination of small geometries and junction depths which would not allow for an accurate approximation. Other considerations such as field lowering effects and effective threshold were excluded because they did not provide additional insight to the extracted mobilities.

6.5.2 Threshold Voltage Extraction

For a very small V_{DS} and a fixed V_{SB}, a graphical method for determining the threshold voltage exists [6,30,31]. The relationship

$$I_{D,lin} = W/L\ \mu\ C'_{ox} V_{DS}(V_{GS}-V_T), \qquad \text{for a very small } V_{DS}, \tag{6.5.3}$$

can be rearranged to yield

$$\Delta I_{DS}/\Delta V_{GS} = W/L\ \mu\ C'_{ox} V_{DS} \qquad (6.5.4)$$

with the intercept equal to the threshold voltage, V_T.

Figure 6.5.1 shows a typical I_{DS} versus V_{GS} curve. For a small V_{DS} value, chosen as 0.5 volts for each case, threshold voltage was determined at the point where the slope of the line intercepted the drain-to-source leakage current threshold. This point is considered to be zero in most cases.

6.5.3 Subthreshold Swing Extraction

The inverse subthreshold slope, or subthreshold swing (SS) can be extracted from the log (I_{DS}) versus V_{GS} curve, as defined in Section 2.2.3 [2,32]. The technique involves sweeping I_{DS} from the pico-Amp range to the milli-Amp range over a gate-to-source voltage that will ensure that the device is either on or off. Figure 6.5.3 shows a typical log (I_{DS}) versus V_{GS} curve with V_{DS} chosen as 5V The V_{DS} voltage was selected by choosing a value which demonstrates no effect on the subthreshold slope. The "linear" portion, or transition region, was fit to a straight line and extrapolated over one decade of drain-to-source current. The corresponding gate-to-source voltage "swing" was measured and recorded, giving the characteristic subthreshold swing value.

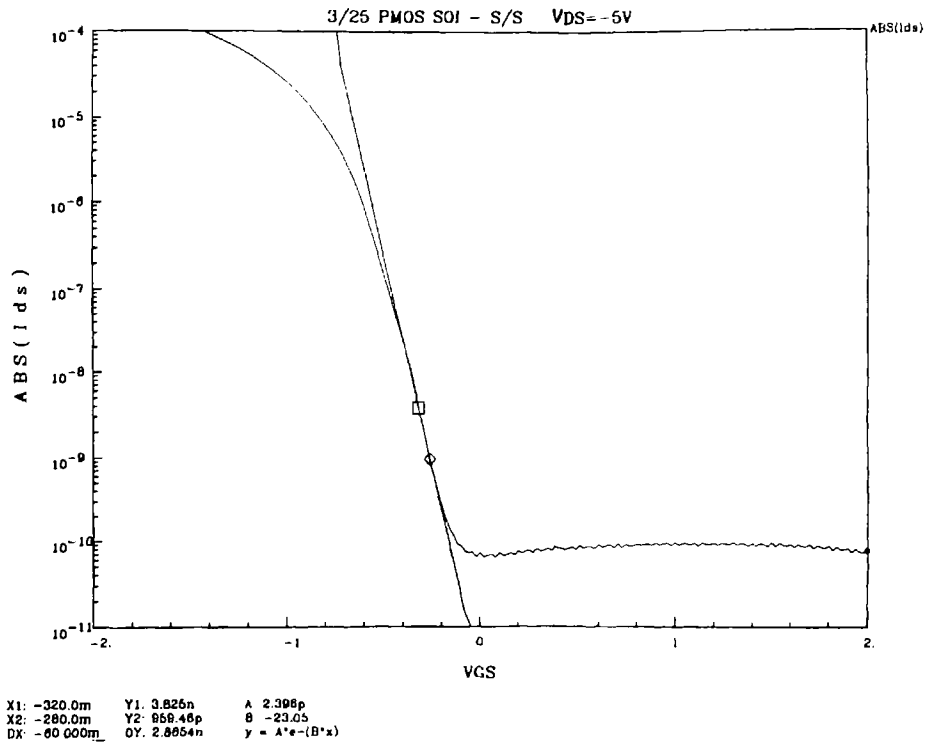

Figure 6.5.3: Log (I_{DS}) versus V_{GS} Curve - Subthreshold Swing

6.5.4 Off-State Leakage Current Extraction

The off-state leakage current was extracted from the subthreshold swing curve, defined in the previous section. With a gate voltage that ensured the device was off, a large negative voltage for NMOS and a large positive voltage for PMOS, the resulting drain-to-source current was recorded. This value indicates how well the device turns off, and is an indicator of the fabrication process integrity.

Chapter 7: Experimental Results

The experimental results can be broken down into experimental values such as effective mobilities, threshold voltages, subthreshold swings, and off-state leakage currents for the NMOS and PMOS bulk-silicon and SOI devices. The discussion of these resulting parameters shows the SOI architecture to be superior for the previously discussed reasons. The data reported represents extraction from over 200 transistors of three different channel lengths and widths for both NMOS and PMOS devices. The three L/W ratios selected were 10/25, 6/25, and 3/25. It was felt that these three combinations would represent long-channel, medium-channel, and short-channel devices, and would provide trends for channel length effects on mobility, subthreshold swing, threshold voltage, and off-state leakage current.

7.1 Device Parameters

7.1.1 SOI Effective Mobilities and Threshold Voltages

SIZE	PMOS			NMOS		
L/W (μm)	$\mu_{h,lin}$ (cm^2/Vs)	$\mu_{h,sat}$ (cm^2/Vs)	V_T (V)	$\mu_{e,lin}$ (cm^2/Vs)	$\mu_{e,sat}$ (cm^2/Vs)	V_T (V)
3/25	422.3	211.2	-1.06	267.9	138.8	**
6/25	448.3	219.3	-0.97	323.7	170.8	**
10/25	427.7	168.9	-1.12	380.6	201.7	**

Table 7.1: SOI Effective Mobilities and Threshold Voltages

Note: Mobilities take lateral diffusion into account by decreasing L by $2X_j$, giving an effective channel length. NMOS threshold voltages were not extracted because of high leakage currents.

$$\mu_{lin,eff.} = \Delta I_{DS}/\Delta V_{GS}\ (L_{eff}/W)\ (1/C'_{ox})\ (1/V_{DS}) \qquad (7.1.1)$$

where $C'_{ox} = 4.7173E\text{-}8\ F/cm^2$

$$\mu_{sat,eff.} = SQRT.(\Delta I_{DS})/\Delta V_{GS}\ (L_{eff}\ /\ W)\ (1/C'_{ox}) \qquad (7.1.2)$$

where $C'_{ox} = 4.71738E\text{-}8\ F/cm^2$

See Appendix D for I_{DS} versus V_{GS} curves from Table 7.1 data.

7.1.2 Single Crystal Effective Mobilities and Threshold Voltages

SIZE	PMOS			NMOS		
L/W (μm)	$\mu_{h,lin}$ (cm^2/Vs)	$\mu_{h,sat}$ (cm^2/Vs)	V_T (V)	$\mu_{e,lin}$ (cm^2/Vs)	$\mu_{e,sat}$ (cm^2/Vs)	V_T (V)
3/25	413.7	28.0	**	393.7	223.1	**
6/25	411.0	31.8	**	404.8	230.5	**
10/25	407.7	17.5	**	421.7	234.1	**

Table 7.2: S.C. Effective Mobilities and Threshold Voltages

Note: Mobilities take lateral diffusion into account by decreasing L by $2X_j$, giving an effective channel length. NMOS and PMOS threshold voltages were not extracted because of high leakage currents.

See Appendix D for I_{DS} versus V_{GS} curves from Table 7.2 data.

7.1.3 SOI Subthreshold Swing and Off-State Leakage Current

SIZE	PMOS		NMOS				
L/W (μm)	S/S (mV/Dec)	$I_{leakage}$ (A)	S/S (mV/Dec)	$I_{leakage}$ (A)	n	C'_{it} (F/cm^2)	D_{it} ($1/cm^2$)
3/25	117.5	3.9E-11	1866.7	4.3E-5			
6/25	160.0	5.0E-11	2333.3	5.2E-5	4.25	9.44E-8	5.8E11
10/25	176.8	3.8E-11	2000.0	3.3E-5	69.50	3.22E-6	2.0E13

Table 7.3: SOI Subthreshold Swing and Off State Leakage Current

$n = SS/\log(10)\,\Phi b$; $\Phi_b = 0.0259$ V

$n = 1 + (C'_b + C'_{it})/C'_{ox}$

$D_{it} = C'_{it}/q$

C'_b = Capacitance between the inversion channel and the back gate electrode.

C'_{it} = Interface trap capacitance per unit area.

D_{it} = The interface trap density

The interface trap density, as calculated above, does not necessarily represent the actual value. The density of interface traps calculated above represents the absolute minimum that the devices can exhibit based solely on the subthreshold swing. The actual density of interface traps may be higher and can be determined by capacitance-voltage measurements. The numbers above are useful as a means of comparison. See Appendix D for log (I_{DS}) versus V_{GS} curves from Table 7.3 data.

7.1.4 Single-Crystal Subthreshold Swing and Off-State Leakage Current

SIZE	PMOS		NMOS				
L/W (μm)	S/S (mV/Dec)	$I_{leakage}$ (A)	S/S (mV/Dec)	$I_{leakage}$ (A)	n	C'_{it} (F/cm^2)	D_{it} ($1/cm^2$)
3/25	> 4000	2.0E-3	1950.0	9.5E-5			
6/25	> 4000	1.0E-3	1500.0	2.0E-5	154.4	7.23E-6	4.5E13
10/25	> 4000	8.5E-4	2100.0	1.0E-5	57.9	2.68E-6	1.7E13

Table 7.4: Single Crystal Subthreshold Swing and Off-State Leakage Current

See Appendix D for log (I_{DS}) versus V_{GS} curves from Table 7.4 data.

7.2 Discussion of Results

First, it is helpful to review some of the best reported device parameters in order to understand how the bonded and etched-back SOI devices compare. The data reported is taken from previous research performed at RIT, and from research originating elsewhere.

Group	Originator	$\mu_{h,lin}$	$\mu_{e,lin}$	S/S	$I_{leakage}$	D_{it}
B-E SOI	B. Dinse	483	474	110	5.0E-12	5.8E-12
S.C.	B. Dinse	414	445	1500	1.0E-5	**
POLYTF	B. Dinse	1.34	0.63	1850	2.0E-9	**
S.C.	D. Hunt [33]	**	**	120	**	**
POLYTF	D. Hunt [33]	27	**	1140	2.0E-10	**
POLYTF	L. Ternullo [28]	66	56	465	**	1.4E12
S.C.	G. Neri [34]	247	444	400	**	**
S.C.	D. Price [35]	170	456	160	**	**
SIMOX	Y. Yamaguchi [36]	150	640	80	**	**
ZMR	L. Thompson [37]	**	823	131	**	**

Table 7.5: Best Reported Device Parameters

** Represents data which was not reported or avaiable.

The most significant factor presented in the table above is that the bonded and etched-back SOI devices consistently report higher hole and electron mobilities and lower subthreshold swings than ever fabricated before at RIT. These results confirm the theories presented throughout earlier sections of this paper.

Another factor presented in Table 7.5 is the relationship between the polysilicon thin-film devices, fabricated using the B-E SOI process, to those fabricated using Ternullo's process. As mentioned earlier, these devices were fabricated to compare the B-E SOI process with Ternullo's and "benchmark" one against the other. Ternullo's

reported mobilities were approximately of the same order of magnitude. Understanding that his process contained grain growth enhancement steps, it is reasonable to say that the two processes match fairly well. This relationship, plus other monitors, shows that the process was not out of the ordinary and gives good confidence that it can be repeated again. Additionally, this points to the SOI structure as being responsible for the enhanced device performance and confirms that the process of fabrication is straight forward and simple.

In comparing the results yielded to those obtained external to RIT, those obtained here are be seen to exhibit subthreshold swings comparable to and mobilities smaller than those obtained elsewhere. This is most likely due to RIT's CMOS process. As seen in Table 7.5, no mobilities higher than those in the presently fabricated SOI devices have been obtained. Future work at RIT should include optimization of this parameter. It is felt that if mobilities are investigated and optimized, values matching or exceeding those outside of RIT could be obtained.

Another result evident from Tables 7.1, 7.2, and 7.3 is inferior NMOS devices. The data indicates a lightly doped, n-type region in the channel. The junctions were investigated and found to account for only tens of nano-Amps of leakage. One possible cause for this result is dopant being driven through the poly gate into the channel. This is unlikely because the models do not support this for the drive time used for poly doping and the additional high-temperature steps. Another possibility could be defects in the silicon, making it n-type. There is no way to verify this with the given analytical equipment and the thoery is not supported by the original materials data. This question still remains unanswered and is being considered with IBM.

Chapter 8: Conclusions

The first single-crystal-silicon-on-insulator MOSFETs fabricated at RIT compare to state of the art devices. A hole mobility of 486 cm^2/V-s was obtained in PMOS SOI, comparable to state-of-the-art, and exceeding any mobility previously reported at RIT. A subthreshold swing of 110mV/decade was observed in PMOS SOI, the best to the author's knowledge at RIT. The NMOS devices were found to be inferior to those fabricated external to RIT using this process.

The present work opens new areas for continued research. First, it is felt that the cause of the poor NMOS performance should be explored. This can include investigation of the channel region's apperent abnormality, junction leakages, and mobilities. Second, it would be helpful to fabricate functional CMOS circuits, such as ring oscillators, to obtain a direct device performance comparison. Another interesting study would be to include the effect of a SiGe channel to substitute results obtained previously by Ternullo []. Smaller geometries and thinner gate oxides could be attempted to study the resulting short-channel effects on both the SOI substrate and single-crystal silicon substrate. Fabricating CMOS devices on SIMOX and/or ZMR substrates and comparing them to the B-E SOI substrate could yield comparisons such as those found in Tables 3.7, 3.8, and 7.1 7.4. Finally, back-channel effects on existing SOI MOSFETs could be explored.

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Appendix A:

SOI Fabrication Process Steps

PROCESS FOLLOWING SUBSTRATE PREPARATION

Mask 1: Mesa

RIE 75 watts 75 mtorr.
SF_6/O_2 30:3 sccm
BE1-4 PS1-3
☛ Used poly control wafer to determine etch rate for poly si
3000Å/min. (45 sec. etch)
☛ Used device wafer to determine etch rate for SOI
Required 40 sec. etch (3000Å/min.)

Strip Resist

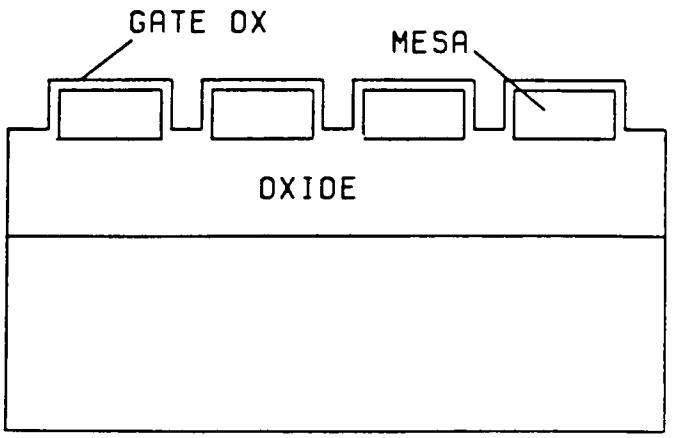
Piranha 3:1 H_2SO_4/H_2O_2 5 min.

RCA Clean

APM 10 min./Rinse/HF dip 10 sec.
HPM 10 min./Rinse/Dry

Gate Oxide Growth

O2 with TCA bubbler (25°C)
O_2 4.0 lpm, TCA N_2 source 189 sccm
Tube clean for 15 min. @ 900°C
Insert wafers 12 in/min.
Ramp 900-1100°C 10/90 O_2/N_2 (0.5/4.5 lpm) 15 min.
Soak 1100°C 4.0 lpm dry O_2 13 min.
Ramp down 1100-900°C 4.5 lpm N_2 30 min.
☛ Included control wafer for gate oxide measurement
732+/-12Å



Polysilicon Deposition (Gate Electrode)

Immedeatly following Gate Ox.
610°C, 60 min.
45% SiH_4, 325mtorr (dep.)
☛ Included 2 1000Å oxide control wafers for polysilicon measurement
5687+/-23Å

Poly Gate Dope

Spin on dopant (Emulsitone N-250)
Spin @3000rpm 10 sec.
Bake @180-190°C 15 min.
Diffusion @900°C 20 min 10/90 O_2/N_2 (0.5/4.5 lpm)
Etch Glass (deglaze) BOE
☛ Sheet resistances: BE: 52.4$^{\Omega}/_{\square}$ SC: 72.0$^{\Omega}/_{\square}$ PS: 52.8$^{\Omega}/_{\square}$

Mask 2: Pattern Gate

RIE (same as isolation etch Param)
90 sec. etch

Strip Resist

Piranha 3:1 H_2SO_4/H_2O_2 5 min.

Mask 3: P+ boron^{11} Source/Drain Implant

$1X10^{15}$ atm/cm^2 35 kev
☛ Included control wafer for future sheet res. measurement

Ash Resist

Mask 4: N+ phosphorous^{31} Source/Drain Implant

$1X10^{15}$ atm/cm^2 60 kev
☛ Included control wafer for future sheet res. measurement

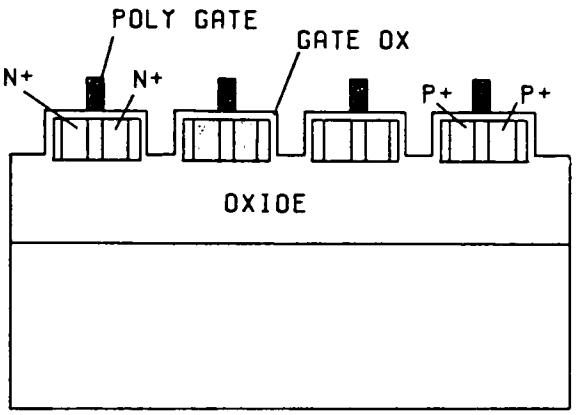
Ash Resist

RCA Clean

APM 10 min./Rinse/HF dip 10 sec.
HPM 10 min./Rinse/Dry

Implant Anneal

Grow ~200 A oxide over gate poly
Soak 900°C 35 min. 5 lpm dry O_2
N+ Sheet Res: $124^{\Omega}/_{\square}$ P+ Sheet Res: $161^{\Omega}/_{\square}$



LTO Deposition - Passivation Oxide

400°C, 80 min.
12% O_2, 20% SiH_4, 344mtorr (dep.)
☛ Included 10 control wafers for thickness measurement
☛ Even with controls and baffels, thickness varied from 1165Å - 1864Å (avg. was 1673Å)

LTO Densification

900°C, dry O_2 5lpm, 10.0 min

Mask 5: Pattern Contacts

Etch Oxide in BOE
2400Å/min. LTO etch rate, 1100Å/min. Gate Ox. etch rate
3.5 min. contact etch

Ash Resist

RCA Clean

APM 10 min./Rinse/HF dip 10 sec.
HPM 10 min./Rinse/Dry

Evaporate Al

4000Å

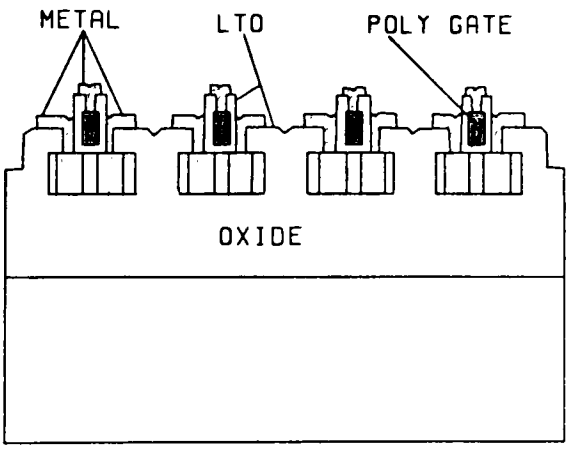
Mask 6: Pattern Al

Etch in Al etch
3 min. (1333Å/min.)

Sinter

450°C, 30min.,5lpm H_2/N_2

Ash Resist



Test

☹ ☹ ☹ ☹ ☹ ☹ ☹ ☹ ☹ ☹ ☹ ☹ ☹

*** DEVICES DON'T WORK ***

Appendix B:

SUPREM III Files

```
USER18:[BPD0667.ATHESIS.SUP3]DSPROF.SUI;3
Title Suprem-3 N+ S/D region
COM          simulated by Brian Dinse
COM          Thesis work 9/10/92 (revision)
Initialize   silicon <100> resistiv boron=8 thickness=2.0 dx=0.02
diffusion    time=15  temperature=800 weto2 T.rate=20
diffusion    time=35  temperature=1100 weto2
diffusion    time=30  temperature=1100 weto2 T.rate=-10
deposit      silicon <100> thicknes=0.195
COM          Using loop to find optimum ox time for
COM          750 A oxide
$ Loop         steps=50 optimize
$    assign    name=tm n.value=20 lower=5 upper=30 optimize
   diffusion  time=16  temperature=900 T.final=1100 F.O2=0.5 F.N2=4.5
   diffusion  time=20 temperature=1100 F.O2=4.0
   diffusion  time=4 temperature=1100 F.O2=4.0 HCL%=4.7
   diffusion  time=4 temperature=1100 F.O2=4.0
$    Argon used in place of N2 for Ramp down
   diffusion  time=34 temperature=1100 T.final=900 F.N2=4.5
$    extract   name=xox thicknes layer=4 target=.075
$ l.end
 deposit      polysilicon temperat=610 pressure=3.5e-4 thicknes=0.5
 diffusion    time=28 temperature=900 ss.phosp
COM          Etching gate polysilicon for S/D region
Etch         polysili
 print       layers
implant      phosphor dose=1E15 energy=60
Extract name=xox1 thickness layer=2
Extract name=xox2 thickness layer=4
Extract name=poly1 thickness layer=3
plot         net active Title="PH Implant before oxide S/D Region"
+            bottom=1e13 top=1e20 device="regis" plot.out="sdphimp.plt"
plot         active phosphorous line=2 color=2 ADD
LABEL  LABEL="Gate Oxide in S/D="@xox2"um" x=1.0 y=1e19
LABEL  LABEL="Si Substrate Thickness="@poly1"um"
LABEL  LABEL="Isolation Oxide="@xox1"um"
LABEL  LABEL="                    "
COM          Oxide growth and S/D anneal at the same time
$ Loop         steps=50 optimize
$    assign    name=tm n.value=20 lower=5 upper=60 optimize
$    diffusion  time=10 temperature=800 t.final=900 F.O2=0.5 F.N2=4.5
   diffusion  time=35 temperature=900          F.O2=5.0
$    diffusion  time=20 temperature=900 t.final=850 F.O2=5.0
$    extract   name=xox thicknes layer=6 target=.04
COM   assign    name=xox1 n.value=@xox target=1000
```

```
$ l.end
electrical steps=1
bias layer=3
end.electrical
Extract  e.resist layer=3 name=rsphd1
Extract name=xox1 thickness layer=2
Extract name=xox3 thickness layer=4
Extract name=poly1 thickness layer=3
print          layers active phosphorous boron concentr x.max=1.0
print          net active concentr x.max=1.0
plot           net active Title="PH Concen, S/D Region"
+             bottom=1e13 top=1e20 device="regis" plot.out="sdphcon.plt"
plot           active phosphorous line=2 color=2 ADD
LABEL   LABEL="Gate Oxide Thick. Aft. Drive="@xox3"um" x=1.0 y=1e19
LABEL   LABEL="Si Substrate Thickness="@poly1"um"
LABEL   LABEL="PH S/D Sheet Res.="@rsphd1"ohm/sqr"
LABEL   LABEL="Isolation Oxide="@xox1"um"
LABEL   LABEL="                    "
deposition      oxide thicknes=0.2 dx=0.02
$ diffusion       time=10 temperature=800 t.final=900 F.O2=2.0 F.N2=2.0
$   Argon was used in place of N2
diffusion       time=10 temperature=900          F.O2=5.0
$ diffusion       time=15 temperature=900 t.final=825 F.O2=4.0
electrical steps=1
bias layer=3
end.electrical
Extract  e.resist layer=3 name=rsphd2
Extract name=xox1 thickness layer=2
Extract name=xox4 thickness layer=4
Extract name=poly1 thickness layer=3
print          layers active phosphorous boron concentr x.max=1.0
print          net active concentr x.max=1.0
plot           net active Title="PH Concen, S/D Region W/LTO + Anneal"
+             bottom=1e13 top=1e20 device="regis" plot.out="sdphlto.plt"
plot           active phosphorous line=2 color=2 ADD
LABEL   LABEL="Gate + Passivation Oxide Thick.="@xox4"um" x=1.0 y=1e19
LABEL   LABEL="Si Substrate Thickness="@poly1"um"
LABEL   LABEL="PH S/D Sheet Res.="@rsphd2"ohm/sqr."
LABEL   LABEL="Isolation Oxide="@xox1"um"
LABEL   LABEL="                    "
Stop
```

```
USER18:[BPD0667.ATHESIS.SUP3]GATENW.SUI;1
Title Suprem-3 Gate Region on SI wafer
COM
COM          simulated by Brian Dinse
COM          Thesis work 7/28/92 (revision)
Initialize     silicon <100> resistiv boron=8 thickness=2.5 dx=0.05
$ Loop          steps=50 optimize
$     assign     name=tm n.value=20 lower=5 upper=30 optimize
    diffusion  time=16  temperature=900 T.final=1100 F.O2=0.5 F.N2=4.5
    diffusion  time=6 temperature=1100 F.O2=4.0
    diffusion  time=3 temperature=1100 F.O2=4.0 HCL%=4.7
    diffusion  time=3 temperature=1100 F.O2=4.0
    diffusion  time=34 temperature=1100 T.final=900 F.N2=4.5
$     extract    name=xox thicknes layer=4 target=.075
COM    assign     name=xox1 n.value=&xox target=1000
$ l.end
deposit        polysilicon temperat=610 pressure=3.5e-4 thicknes=0.5
COM    Using solid solubility to predict Spin on dopant activity
diffusion      time=20 temperature=900 ss.phosp
COM    Standard S/D boron implant
print  layers
implant        phosphor dose=1E15 energy=45
Electrical steps=1
bias layer=3
end.electrical
Extract e.resist layer=3 name=rspdw
Extract name=xox1 thicknes layer=2
Extract name=poly2 thicknes layer=3
plot           net active Title="SI Wafer Gate Con. After PH Implant"
+             bottom=1e13 top=1e20 device="regis" plot.out="wphimpgate.plt"
plot           active phosphorous line=2 color=2 ADD
LABEL  LABEL="Gate Thickness="&poly2"um" x=1.0 Y=1e19
LABEL  LABEL="Gate Sheet Resistance="&rspdw"ohm/sqr."
LABEL  LABEL="Gate Oxide Thickness="&xox1"um"
LABEL  LABEL="              "
COM    Performing oxide growth and S/D anneal at the same time
$ Loop          steps=50 optimize
$     assign     name=tm n.value=20 lower=5 upper=40 optimize
$     diffusion  time=10 temperature=800 t.final=900 F.O2=0.5 F.N2=4.5
   diffusion  time=45 temperature=900          F.O2=4.0
$     diffusion  time=15 temperature=900 t.final=800 F.O2=5.0
$     extract    name=xox thicknes layer=6 target=.04
COM    assign     name=xox1 n.value=&xox target=1000
$ l.end
Electrical steps=1
```

```
bias layer=3
end.electrical
Extract e.resist layer=3 name=rspdw2
Extract name=xox1 thicknes layer=2
Extract name=poly2 thicknes layer=3
Extract name=xox2 thicknes layer=4
print   layers   active phosphorous boron concentr x.max=1.0
print           net active concentr x.max=1.0
plot            net active Title="Si Wafer Ph Concen, Gate Region"
+              bottom=1e13 top=1e20 device="regis" plot.out="wphcongate.plt"
plot            active phosphorous line=2 color=2 ADD
LABEL   LABEL="Thin Isolation Oxide="&xox2"um" x=0.2 y=1e19
LABEL   lx.start=0.2 ly.start=1e19 lx.finis=0.0 ly.finis=1e19 arrow
LABEL   LABEL="Gate Thickness="&poly2"um" x=1.0 y=5e18
LABEL   LABEL="Gate Sheet Resistance="&rspdw2"ohm/sqr."
LABEL   LABEL="Gate Oxide Thickness="&xox1"um"
LABEL   LABEL="              "
deposition      oxide thicknes=0.2 dx=.02
$ diffusion       time=10 temperature=800 t.final=900 F.O2=2.0 F.N2=2.0
diffusion       time=15 temperature=900          F.O2=2.0 F.N2=2.0
$ diffusion       time=15 temperature=900 t.final=825 F.O2=4.0
Electrical steps=1
bias layer=3
end.electrical
Extract e.resist layer=3 name=rspdw3
Extract name=xox1 thicknes layer=2
Extract name=poly2 thicknes layer=3
Extract name=xox3 thicknes layer=4
print   layers   active phosphorous boron concentr x.max=1.0
print           net active concentr x.max=1.0
plot            net active Title="Si Wafer Ph Concen, Gate Region W/LTO"
+              bottom=1e13 top=1e20 device="regis" plot.out="wphltogate.plt"
plot            active phosphorous line=2 color=2 ADD
LABEL   LABEL="Passivation LTO Oxide="&xox3"um" x=1.0 y=1e19
LABEL   LABEL="Gate Thickness="&poly2"um"
LABEL   LABEL="Gate Sheet Resistance="&rspdw3"ohm/sqr."
LABEL   LABEL="Gate Oxide Thickness="&xox1"um"
LABEL   LABEL="              "
Stop
```

```
USER18:[BPD0667.ATHESIS.SUP3]GATEP.SUI;1
Title Suprem-3 P+ S/D Implant
COM
COM          simulated by Brian Dinse
COM          Thesis work 9/29/92 (revision)
Initialize     silicon <100> resistiv boron=8 thickness=2.0 dx=0.05
diffusion      time=15  temperature=800 weto2 T.rate=20
diffusion      time=50  temperature=1100 weto2
diffusion      time=30  temperature=1100 weto2 T.rate=-10
deposit        polysilicon temperat=610 pressure=3.5e-4 thicknes=0.195
COM          Using loop to find optimum ox time for
COMm           750 A oxide
COM
$ Loop          steps=50 optimize
$     assign     name=tm n.value=20 lower=5 upper=30 optimize
diffusion  time=16  temperature=900 T.final=1100 F.O2=0.5 F.N2=4.5
   diffusion  time=20 temperature=1100 F.O2=4.0
   diffusion  time=3 temperature=1100 F.O2=4.0 HCL%=4.7
   diffusion  time=3 temperature=1100 F.O2=4.0
$     Actually using Argon NOT N2 in ramp down to help tie up
$     some surface states.
   diffusion  time=34 temperature=1100 T.final=900 F.N2=4.5
$     extract    name=xox thicknes layer=4 target=.075
COM    assign     name=xox1 n.value=@xox target=1000
$ l.end
deposit        polysilicon temperat=610 pressure=3.5e-4 thicknes=0.5
COM    Using solid solubility to predict Spin on dopant activity
diffusion      time=20 temperature=900 ss.phosp
COM    Standard S/D boron implant
print  layers
implant        boron dose=1E15 energy=35
electrical steps=1
bias  layer=5
end.electrical
Extract  e.resist name=rsbd layer=5
Extract  name=xox2 thicknes layer=4
Extract  name=xox1 thicknes layer=2
Extract  name=poly2 thicknes layer=5
Extract  name=poly1 thicknes layer=3
plot          net active Title="Conc. SS.Phos. After Predep and B Implant"
+            bottom=1e13 top=1e20 device="regis" plot.out="phbimpgate.plt"
plot          active phosphorous line=2 color=2 ADD
plot          chemical boron line=3 color=3 ADD
LABEL  LABEL="Gate Thickness="@poly2"um" x=1.0 y=1e19
LABEL  LABEL="Gate Sheet Resistance="@rsbd"ohm/sqr."
```

```
LABEL   LABEL="Gate Oxide Thickness="@xox2"um"
LABEL   LABEL="Poly Substrate Thickness="@poly1"um"
LABEL   LABEL="Thick Isolation Oxide="@xox1"um"
LABEL   LABEL="              "
COM     Performing oxide growth and S/D anneal at the same time
$ Loop          steps=50 optimize
$       assign      name=tm n.value=20 lower=5 upper=50 optimize
$       diffusion   time=10 temperature=800 t.final=900 F.O2=0.5 F.N2=4.5
    diffusion   time=35 temperature=900          F.O2=5.0
$       diffusion   time=15 temperature=900 t.final=800 F.O2=5.0
$ extract     name=xox thicknes layer=6 target=.02
COM     assign      name=xox1 n.value=@xox target=1000
$ l.end
electrical steps=1
bias  layer=5
end.electrical
Extract   e.resist name=rsbd2 layer=5
Extract   name=xox3 thicknes layer=6
Extract   name=xox2 thicknes layer=4
Extract   name=xox1 thicknes layer=2
Extract   name=poly2 thicknes layer=5
Extract   name=poly1 thicknes layer=3
print   layers   active phosphorous boron concentr x.max=1.0
print           net active concentr x.max=1.0
plot            net active Title="Ph & B Concen, Gate Region"
+               bottom=1e13 top=1e20 device="regis" plot.out="phbcongate.plt"
plot            active phosphorous line=2 color=2 ADD
plot            active boron line=3 color=3 ADD
LABEL   LABEL="Thin Isolation Oxide="@xox3"um" x=0.2 y=1e19
LABEL   lx.start=0.2 ly.start=1e19 lx.finis=0.0 ly.finis=1e19 arrow
LABEL   LABEL="Gate Thickness="@poly2"um" x=1.0 y=5e18
LABEL   LABEL="Gate Sheet Resistance="@rsbd2"ohm/sqr."
LABEL   LABEL="Gate Oxide Thickness="@xox2"um"
LABEL   LABEL="Poly Substrate Thickness="@poly1"um"
LABEL   LABEL="Thick Isolation Oxide="@xox1"um"
LABEL   LABEL="              "
deposition      oxide thicknes=0.2 dx=.02
$ diffusion       time=10 temperature=800 t.final=900 F.O2=2.0 F.N2=2.0
$   Actually using Argon Not N2 for Ramp down.
diffusion       time=10 temperature=900          F.O2=5.0
$ diffusion       time=15 temperature=900 t.final=825 F.O2=4.0
electrical steps=1
bias  layer=5
end.electrical
Extract   e.resist name=rsbd3 layer=5
```

```
Extract   name=xox4 thicknes layer=6
Extract   name=xox2 thicknes layer=4
Extract   name=xox1 thicknes layer=2
Extract   name=poly2 thicknes layer=5
Extract   name=poly1 thicknes layer=3
print   layers   active phosphorous boron concentr x.max=1.0
print            net active concentr x.max=1.0
plot             net active Title="Final Profile of Ph and B; PMOS Gate"
+         bottom=1e13 top=1e20 device="l/postscript" plot.out="phbltogate.plt"
plot             active phosphorous line=2 color=2 ADD
plot             active boron line=3 color=3 ADD
LABEL   LABEL="Passivation LTO Oxide="@xox4"um" x=1.0 y=1e19
LABEL   LABEL="Gate Thickness="@poly2"um"
LABEL   LABEL="Gate Sheet Resistance="@rsbd3"ohm/sqr."
LABEL   LABEL="Gate Oxide Thickness="@xox2"um"
LABEL   LABEL="Poly Substrate Thickness="@poly1"um"
LABEL   LABEL="Thick Isolation Oxide="@xox1"um"
LABEL   LABEL="                  "
LABEL   LABEL="                  "
LABEL   LABEL="Boron Concentration Profile "
Stop
```

```
USER18:[BPD0667.ATHESIS.SUP3]GATEPW.SUI;1
Title Suprem-3 Gate Region SI wafer
COM          simulated by Brian Dinse
COM          Thesis work 7/28/92 (revision)
Initialize     silicon <100> resistiv boron=8 thickness=2.5 dx=0.05
$ Loop          steps=50 optimize
$     assign     name=tm n.value=20 lower=5 upper=30 optimize
diffusion  time=16  temperature=900 T.final=1100 F.O2=0.5 F.N2=4.5
   diffusion  time=6 temperature=1100 F.O2=4.0
   diffusion  time=3 temperature=1100 F.O2=4.0 HCL%=4.7
   diffusion  time=3 temperature=1100 F.O2=4.0
$     N2 flow was replaced with Argon
   diffusion  time=34 temperature=1100 T.final=900 F.N2=4.5
$     extract    name=xox thicknes layer=4 target=.075
COM    assign     name=xox1 n.value=&xox target=1000
$ l.end
deposit        polysilicon temperat=610 pressure=3.5e-4 thicknes=0.5
COM    Using solid solubility to predict Spin on dopant activity
diffusion      time=20 temperature=900 ss.phosp
COM    Standard S/D boron implant
print  layers
implant        boron dose=1E15 energy=35
Electrical steps=1
bias layer=3
end.electrical
Extract e.resist layer=3 name=rspdw
Extract name=xox1 thicknes layer=2
Extract name=poly2 thicknes layer=3
plot           net active Title="SI Wafer Gate Con. After B Implant"
+              bottom=1e13 top=1e20 device="regis" plot.out="wbimpgate.plt"
plot           active phosphorous line=2 color=2 ADD
plot           active boron line=3 color=3 ADD
LABEL  LABEL="Gate Thickness="&poly2"um" x=1.0 Y=1e19
LABEL  LABEL="Gate Sheet Resistance="&rspdw"ohm/sqr."
LABEL  LABEL="Gate Oxide Thickness="&xox1"um"
LABEL  LABEL="                "
COM    Performing oxide growth and S/D anneal at the same time
$ Loop          steps=50 optimize
$     assign     name=tm n.value=20 lower=5 upper=40 optimize
$     diffusion  time=10 temperature=800 t.final=900 F.O2=0.5 F.N2=4.5
   diffusion  time=45 temperature=900          F.O2=4.0
$     diffusion  time=15 temperature=900 t.final=800 F.O2=5.0
$     extract    name=xox thicknes layer=6 target=.04
COM    assign     name=xox1 n.value=&xox target=1000
$ l.end
```

```
Electrical steps=1
bias layer=3
end.electrical
Extract e.resist layer=3 name=rspdw2
Extract name=xox1 thicknes layer=2
Extract name=poly2 thicknes layer=3
Extract name=xox2 thicknes layer=4
print   layers   active phosphorous boron concentr x.max=1.0
print          net active concentr x.max=1.0
plot           net active Title="Si Wafer PH/B Concen, Gate Region"
+             bottom=1e13 top=1e20 device="regis" plot.out="wbcongate.plt"
plot           active phosphorous line=2 color=2 ADD
plot           active boron line=3 color=3 ADD
LABEL   LABEL="Thin Isolation Oxide="&xox2"um" x=0.2 y=1e19
LABEL   lx.start=0.2 ly.start=1e19 lx.finis=0.0 ly.finis=1e19 arrow
LABEL   LABEL="Gate Thickness="&poly2"um" x=1.0 y=5e18
LABEL   LABEL="Gate Sheet Resistance="&rspdw2"ohm/sqr."
LABEL   LABEL="Gate Oxide Thickness="&xox1"um"
LABEL   LABEL="              "
deposition      oxide thicknes=0.2 dx=.02
$ diffusion       time=10 temperature=800 t.final=900 F.O2=2.0 F.N2=2.0
$   N2 flow replace with Argon
diffusion       time=15 temperature=900          F.O2=2.0 F.N2=2.0
$ diffusion       time=15 temperature=900 t.final=825 F.O2=4.0
Electrical steps=1
bias layer=3
end.electrical
Extract e.resist layer=3 name=rspdw3
Extract name=xox1 thicknes layer=2
Extract name=poly2 thicknes layer=3
Extract name=xox3 thicknes layer=4
print   layers   active phosphorous boron concentr x.max=1.0
print          net active concentr x.max=1.0
plot           net active Title="Si Wafer B Concen, Gate Region W/LTO"
+             bottom=1e13 top=1e20 device="regis" plot.out="wbltogate.plt"
plot           active phosphorous line=2 color=2 ADD
plot           active boron line=3 color=3 ADD
LABEL   LABEL="Passivation LTO Oxide="&xox3"um" x=1.0 y=1e19
LABEL   LABEL="Gate Thickness="&poly2"um"
LABEL   LABEL="Gate Sheet Resistance="&rspdw3"ohm/sqr."
LABEL   LABEL="Gate Oxide Thickness="&xox1"um"
```

```
USER18:[BPD0667.ATHESIS.SUP3]XOX1.SUI;1
Title Suprem-3 (1000 A)xox
COM          1000 A oxide grow for poly measurement
COM          simulated by Brian Dinse
COM          Thesis work 6/26/92 (revision)
Initialize   silicon <100> resistiv boron=8 thickness=2.0 dx=0.05
COM          Using loop to find optimum ox time for
COMm           1000 A oxide
COM
Loop         steps=100 optimize
   assign    name=tm n.value=20 lower=5 upper=32 optimize
diffusion  time=17  temperature=900 T.final=1100 F.O2=0.5 F.N2=4.5
   diffusion  time=&tm temperature=1100 F.O2=4.0 HCL%=3
   diffusion  time=34 temperature=1100 T.final=900 F.N2=4.5
   extract    name=xox thicknes layer=2 target=.061
COM   assign     name=xox1 n.value=&xox target=1000
l.end
Stop
```

```
USER18:[BPD0667.ATHESIS.SUP3]XOX5.SUI;1
Title Suprem-3 (1000 A)xox
COM          1000 A oxide grow for poly measurement
COM          simulated by Brian Dinse
COM          Thesis work 6/26/92 (revision)
Initialize   silicon <100> resistiv boron=8 thickness=2.0 dx=0.05
COM          Using loop to find optimum ox time for
COMm           1000 A oxide
COM
Loop         steps=100 optimize
  assign     name=tm n.value=65 lower=40 upper=90 optimize
diffusion  time=15  temperature=800 weto2 T.rate=13.3
  diffusion  time=&tm temperature=1000 weto2
  diffusion  time=15 temperature=1000 weto2 T.rate=-13.3
  extract    name=xox thicknes layer=2 target=.5
COM   assign     name=xox1 n.value=&xox target=1000
l.end
Stop
```

```
USER18:[BPD0667.ATHESIS.SUP3]XOXPOLY.SUI;1
Title Suprem-3 channels (1000 A)xox
COM          1000 A oxide grow for poly measurement
COM          simulated by Brian Dinse
COM          Thesis work 6/26/92 (revision)
Initialize     silicon <100> resistiv boron=8 thickness=2.0 dx=0.05
diffusion      time=15  temperature=800 weto2 T.rate=20
diffusion      time=50  temperature=1100 weto2
diffusion      time=30  temperature=1100 weto2 T.rate=-10
deposit        polysilicon temperat=610 pressure=3.5e-4 thicknes=0.195
COM            Using loop to find optimum ox time for
COMm             1000 A oxide
Loop          steps=50 optimize
   assign     name=tm n.value=20 lower=5 upper=30 optimize
    diffusion  time=15  temperature=800 T.final=1100 F.O2=0.5 F.N2=4.5
   diffusion  time=&tm temperature=1100 F.O2=4.0 HCL%=3
   diffusion  time=35 temperature=950 T.final=850 F.N2=4.0
   extract    name=xox thicknes layer=4 target=.075
COM    assign     name=xox1 n.value=&xox target=1000
l.end
deposit        polysilicon temperat=610 pressure=3.5e-4 thicknes=0.5
diffusion      time=20 temperature=900 ss.phosp
print          active phosphorous concentr layer=5 x.max=1.0
plot           net active Title="Conc. SS.Phos. after predep"
+             bottom=1e13 top=1e20 device="regis" plot.out="phoscon.plt"
plot           active phosphorous line=2 color=2 ADD
implant          boron dose=1E15 energy=30
plot           net active Title="Conc. SS.Phos. After Predep and B Implant"
+             bottom=1e13 top=1e20 device="regis" plot.out="phwbimp.plt"
plot           active phosphorous line=2 color=2 ADD
plot           chemical boron line=3 color=3 ADD
Loop            steps=50 optimize
   assign     name=tm n.value=20 lower=5 upper=30 optimize
diffusion   time=15 temperature=800 t.final=1000 F.O2=0.5 F.N2=4.5
   diffusion  time=&tm temperature=1000          F.O2=5.0
   diffusion  time=25 temperature=1000 t.final=850 F.O2=5.0
   extract    name=xox thicknes layer=6 target=.04
COM    assign     name=xox1 n.value=&xox target=1000
l.end
print          active phosphorous boron concentr x.max=1.0
print          net active concentr x.max=1.0
plot           net active phosphorous Title="Ph & B Concen, Gate Region"
+             bottom=1e13 top=1e20 device="regis" plot.out="phwbcon.plt"
```

```
USER18:[BPD0667.ATHESIS.SUP4]LATDIFF.IN;1
$ TMA TSUPREM4 RIT-SCN CMOS NMOS enhancement transistor simulation
COMMENT  DATE          6/10/92
COMMENT  FILENAME      LATDIFFP.IN
COMMENT  FILES CREATED  LATDIFFP.STR  SUPREM IV structure file
COMMENT  FILES USED     NONE
COMMENT  CREATED BY     LUIGI TERNULLO
COMMENT  PURPOSE        NMOS device of SCN CMOS
COMMENT
$
$ MASK LEVELS  xxxx - opaque    ---- clear
$
$ x axis - um 0---1---2---3---4---5---6---7---8---9--10--11--12--13--14
$
$ N+ DIFF     xxxxxxxxxxxxxxxxx-------------------------------------
$           NMOS device is not in the well
$ active      xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx--------
$ fieldvt     ------------------------------------------------------
$           only the nwell is covered, totally clear for NMOS
$ poly        xxxxxxxxx-----------------------------------------------
$ pselect     xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
$           NMOS devices covered, not implanted, PMOS implanted
$ not pselect ------------------------------------------------------
$           NMOS devices implanted
$ contact     xxxxxxxxxxxxxxxxxxxxxxxx---------------xxxxxxxxxxxxxxx
$ metal1      ----------------xxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxxx
$ via         not simulated
$ metal2      not simulated
$ passivation not simulated
$
$ Define the grid
$
$   Note: The following "DEFINE" statement sets the grid density for the
$         simulation.  A larger value of "GDENS" gives a denser grid.
$         A value of 1 is used for setting up the simulation; 2 is used
$         for most of the simulation work, while values of 3 or greater
$         are used to get the final answers.

DEFINE    GDENS  1

$   Specify the horizontal grid spacings at various x values
LINE  X   LOCATION=0.0    SPACING=(0.2/ GDENS )
LINE  X   LOCATION=3.0    SPACING=(0.2/ GDENS )
LINE  X   LOCATION=4.0    SPACING=(0.5/ GDENS )
LINE  X   LOCATION=6.0    SPACING=(0.5/ GDENS )
```

```
$  LINE X  LOCATION=11.0  SPACING=(0.2/ GDENS )
$  LINE X  LOCATION=14.0  SPACING=(0.2/ GDENS )
$  Specify the vertical grid spacings at various y values
LINE Y  LOCATION=0.0  SPACING=(0.2/ GDENS )
LINE Y  LOCATION=1.0  SPACING=(0.2/ GDENS )
$  LINE Y  LOCATION=10.0  SPACING=(2.0/ GDENS )
$ Tailor the grid to the device being simulated
$  Eliminate horizontal grid lines below the active device
$  Eliminate vertical grid lines deep in the substrate
$ ELIMINATE COLUMNS Y.MIN=2.0
$ ELIMINATE COLUMNS Y.MIN=3.0
$ ELIMINATE COLUMNS Y.MIN=4.0
$ Initialize the structure
INITIALIZE <100> BORON=8E15
OPTION   DEVICE=REGIS
$SELECT   TITLE="RIT-SCN CMOS, NMOS - Initial Grid"
$PLOT.2D   SCALE GRID Y.MAX=6.0
$ Initial well masking and alignment oxidation
METHOD   COMPRESS
DIFFUSION TIME=10 TEMP=1000  F.O2=6.0 F.N2=1.0
DIFFUSION TIME=65 TEMP=1100  F.O2=2.0 F.H2O=3.0
DIFFUSION TIME=5  TEMP=1000  F.O2=7.0 F.N2=1.0
DIFFUSION TIME=15 TEMP=1000  F.N2=5.0
$  DIFFUSION TIME=780 TEMP=1150  F.N2=5.0
$ Do well photolithography (NMOS device COMpletely covered)
$ DEPOSIT  PHOTORESIST THICKNESS=1.2
DEPOSIT  POLYSILI  THICKNESS=0.2 SPACES=GDENS
DIFFUSION TIME=15 TEMP=800 T.FINAL=1100 F.O2=O.5 F.N2=4.5
DIFFUSION TIME=12 TEMP=1100          F.O2=4.0 HCL=3
DIFFUSION TIME=20 TEMP=1100 T.FINAL=800  F.N2=4.0
DEPOSIT  POLYSILI  THICKNESS=0.5  SPACES=GDENS
ETCH     POLYSILI  LEFT P1.X=4.5
DIFFUSION TIME=15 TEMP=800 T.FINAL=1000 F.O2=O.5 F.N2=4.5
DIFFUSION TIME=20 TEMP=1000          F.O2=4.0
DIFFUSION TIME=15 TEMP=1000 T.FINAL=800  F.N2=4.0
DEPOSIT  NITRIDE  THICKNESS=0.08 SPACES=GDENS
$ DEPOSIT  PHOTORESIST THICKNESS=1.2
$ ETCH    PHOTORESIST START X=1.5 Y=-5.0
$ ETCH    PHOTORESIST CONT  X=1.5 Y=5.0
$ ETCH    PHOTORESIST CONT  X=4.5 Y=5.0
$ ETCH    PHOTORESIST END   X=4.5 Y=-5.0
IMPLANT   BORON DOSE=1.0E15 ENERGY=85
DIFFUSION TIME=10 TEMP=800 T.FINAL=900 F.N2=4.0
DIFFUSION TIME=45 TEMP=900  F.N2=4.0
DIFFUSION TIME=10 TEMP=900 T.FINAL=800 F.N2=4.0
```

```
SELECT    Z=BORON-8E13
PRINT.1D  LAYERS  X.VALUE=3.5
$
$ DEPOSIT   PHOTORESIST  THICKNESS=1.2
$
$ ETCH     NITRIDE     RIGHT  P1.X=12.0
$ SELECT    Z=BORON-8E14
$ PRINT.1D  LAYERS  X.VALUE=14.0
$ PRINT.1D  LAYERS  X.VALUE=0.0
$
$ Plot the initial SCN NMOS structure
SELECT    Z=LOG10(BORON)  TITLE="CMOS TFT, PMOS LATERAL
DIFFUSION"
PLOT.2D   SCALE  Y.MAX=1.0
FOREACH   X  (15 TO 20 STEP 0.5)
 CONTOUR   VALUE=X  LINE=2
END
PAUSE
$ This structure file can be used for SCN NMOS enh.
STRUCTURE  OUTFILE=LATDIFFP.STR

STOP
```

Appendix C:

Contact Rework Process

CONTACT REWORK PROCESS 1

Strip Al - Al etch

RCA Clean
APM 10 min./Rinse/HF dip 10 sec.
HPM 10 min./Rinse/Dry

Mask 5: Pattern Contacts
RIE 75 watts 75 mtorr
SF_6/O_2 30:3 sccm
15 sec.

Etch Oxide
4 min.

Ash Resist

RCA Clean
APM 10 min./Rinse/HF dip 10 sec.
HPM 10 min./Rinse/Dry

Sputter Al
1500 watts, 9E-6Torr base pressure
5000Å

Mask 6: Pattern Al
Etch in Al etch
3.5 min. (1428Å/min.)

Sinter
450°C, 30min. 5lpm H_2/N_2

Test

CONTACT REWORK PROCESS 2

Strip Al - Al etch

RCA Clean
APM 10 min./Rinse/HF dip 10 sec.
HPM 10 min./Rinse/Dry

Grow Oxide
900°C Wet O_2, 20min.
350Å

Mask 5: Pattern Contacts
Etch Oxide
3.5 min.

Ash Resist

RCA Clean
APM 10 min./Rinse/HF dip 10 sec.
HPM 10 min./Rinse/Dry

Sputter Al
1500 watts, 9E-6Torr base pressure
5000Å

Mask 6: Pattern Al
Etch in Al etch
3.5 min. (1428Å/min.)

Sinter
450°C, 30min. 5lpm H_2/N_2

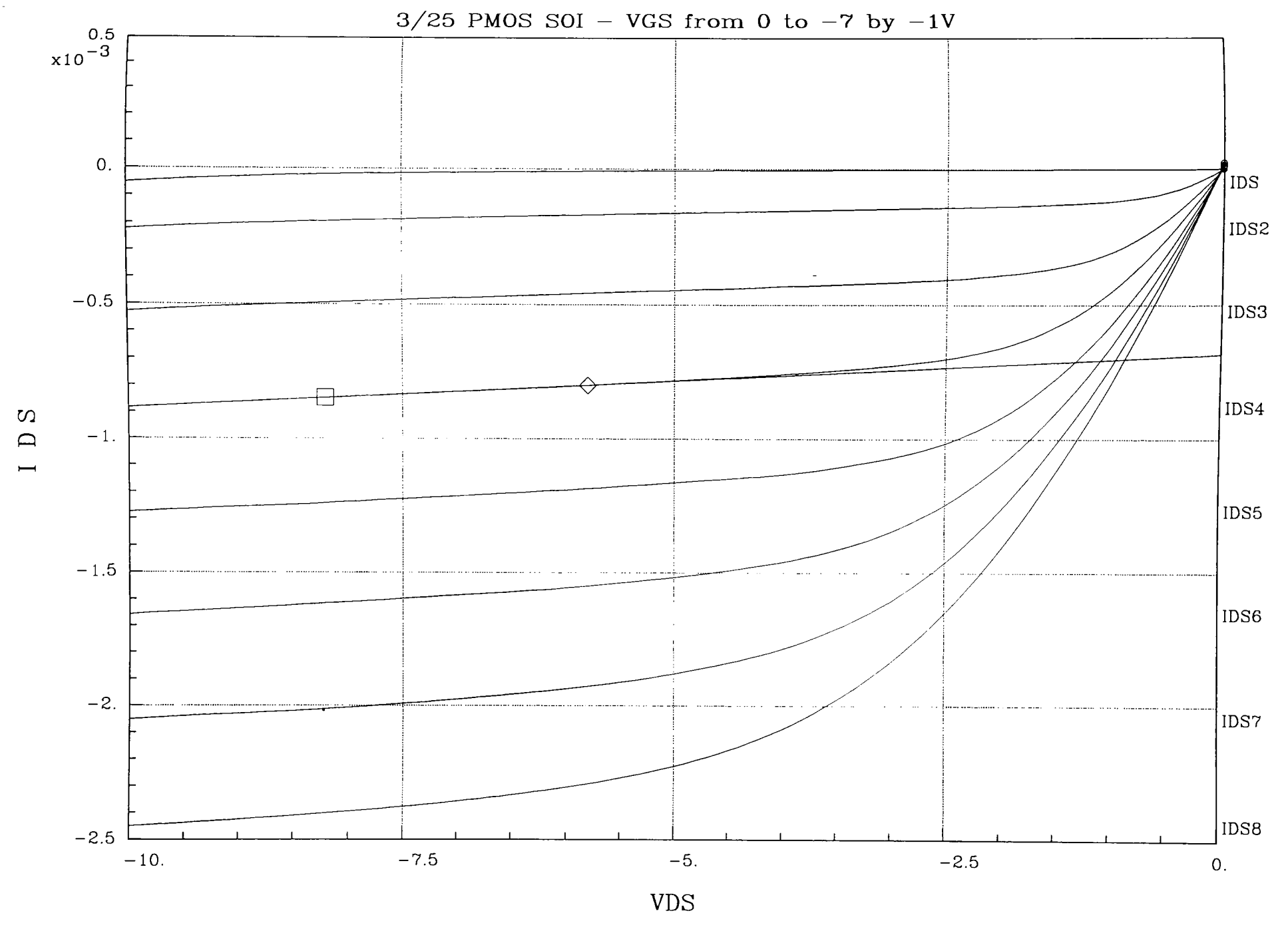
Test

Appendix D:

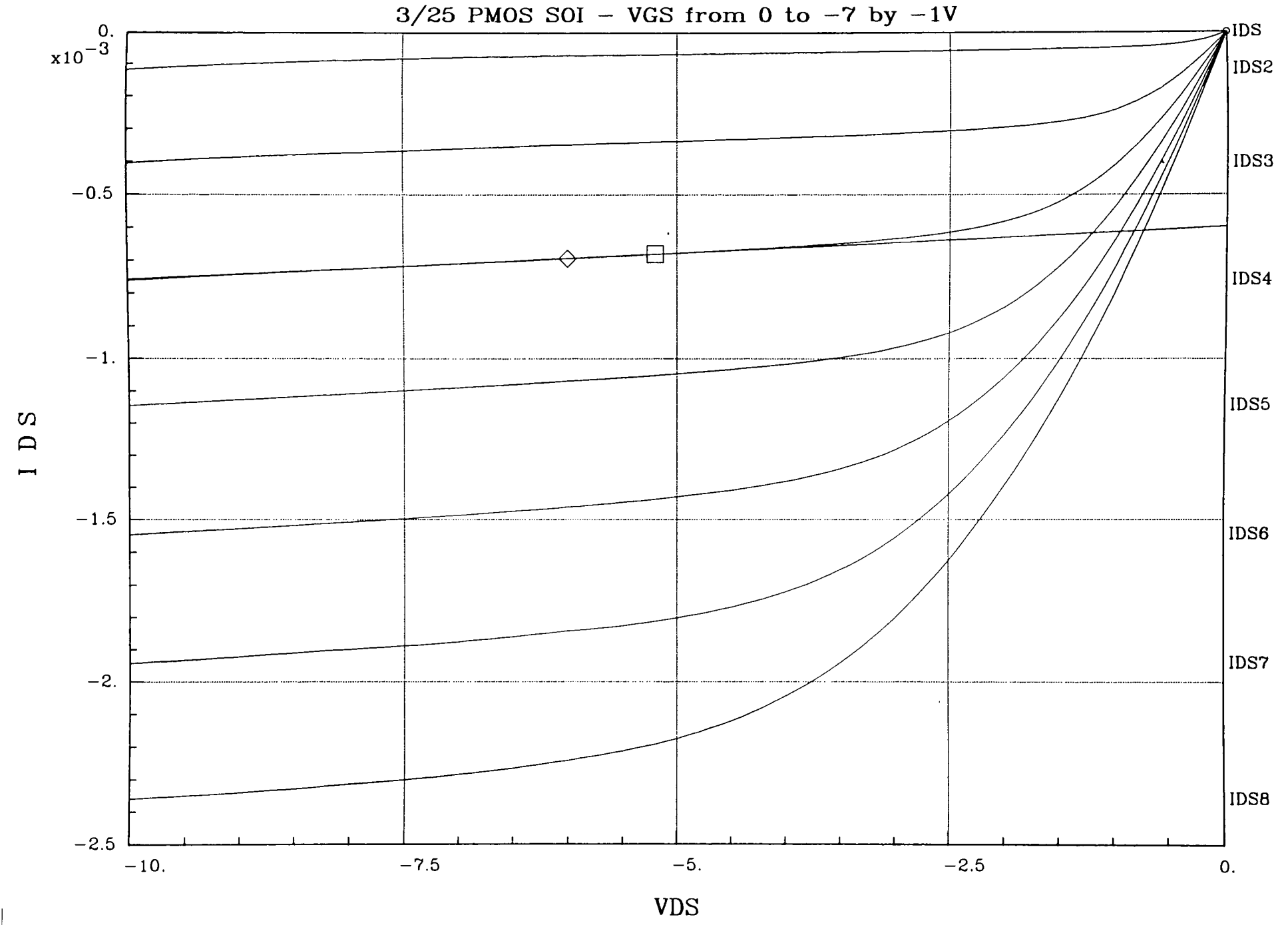
Device Parameter Extraction Curves

PMOS SOI

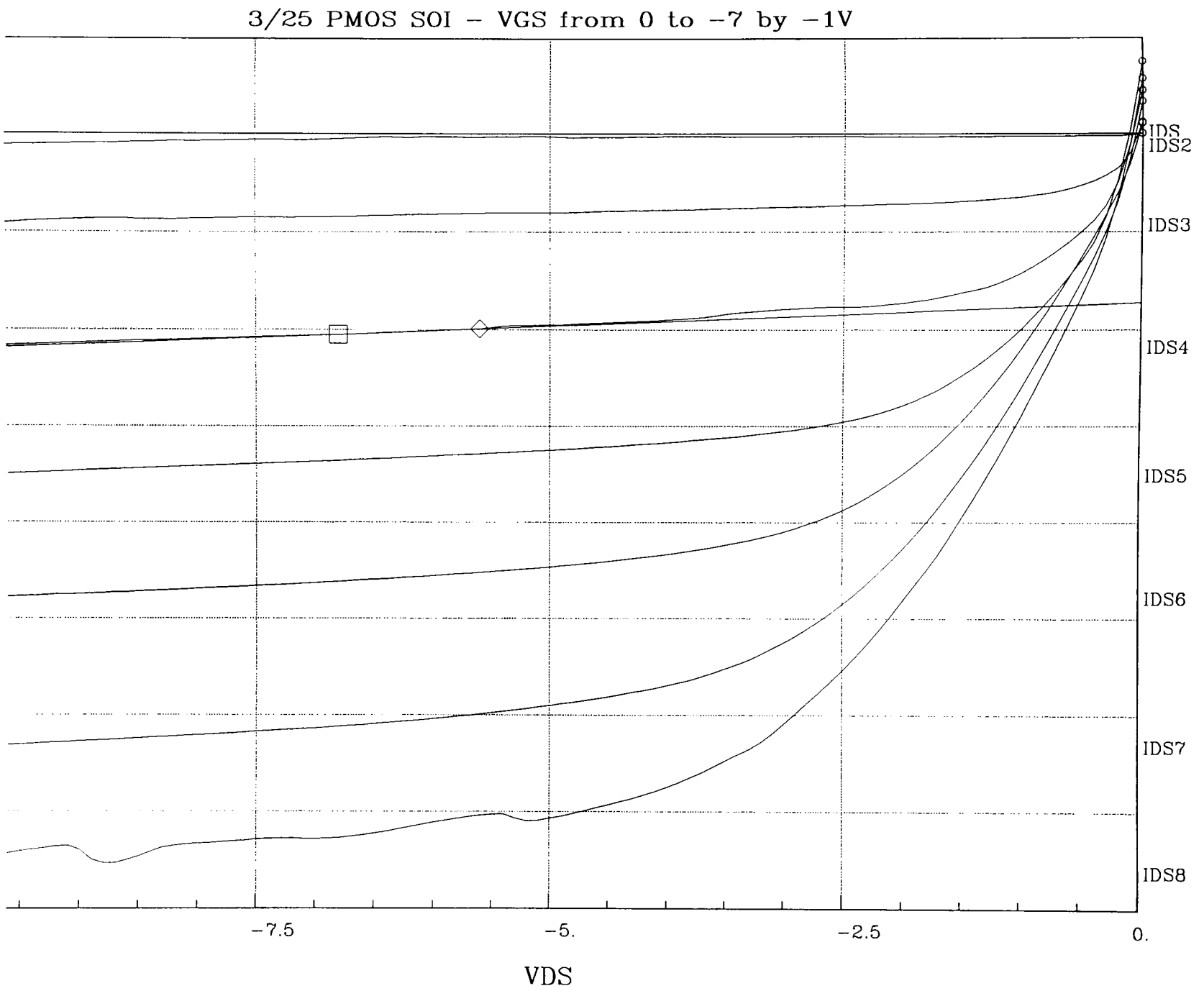
Device Parameter Extraction Curves



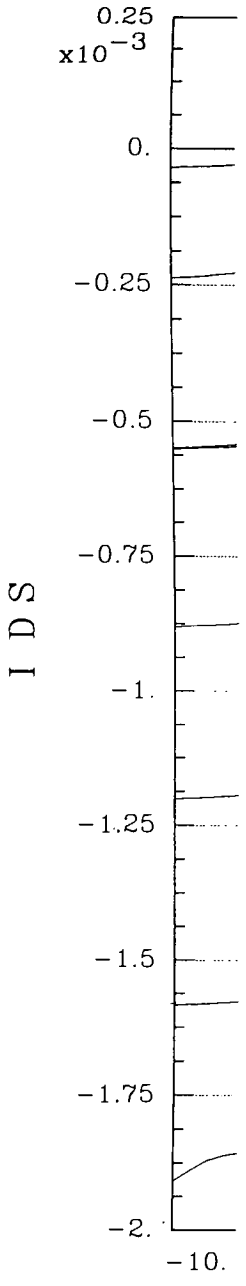
X1: −5.8000 Y1: −799.86u Slope: 19.96u
X2: −8.200 Y2: −847.77u Y−int: −684.10u
DX: 2.400 DY: 47.900u X−int: 34.277



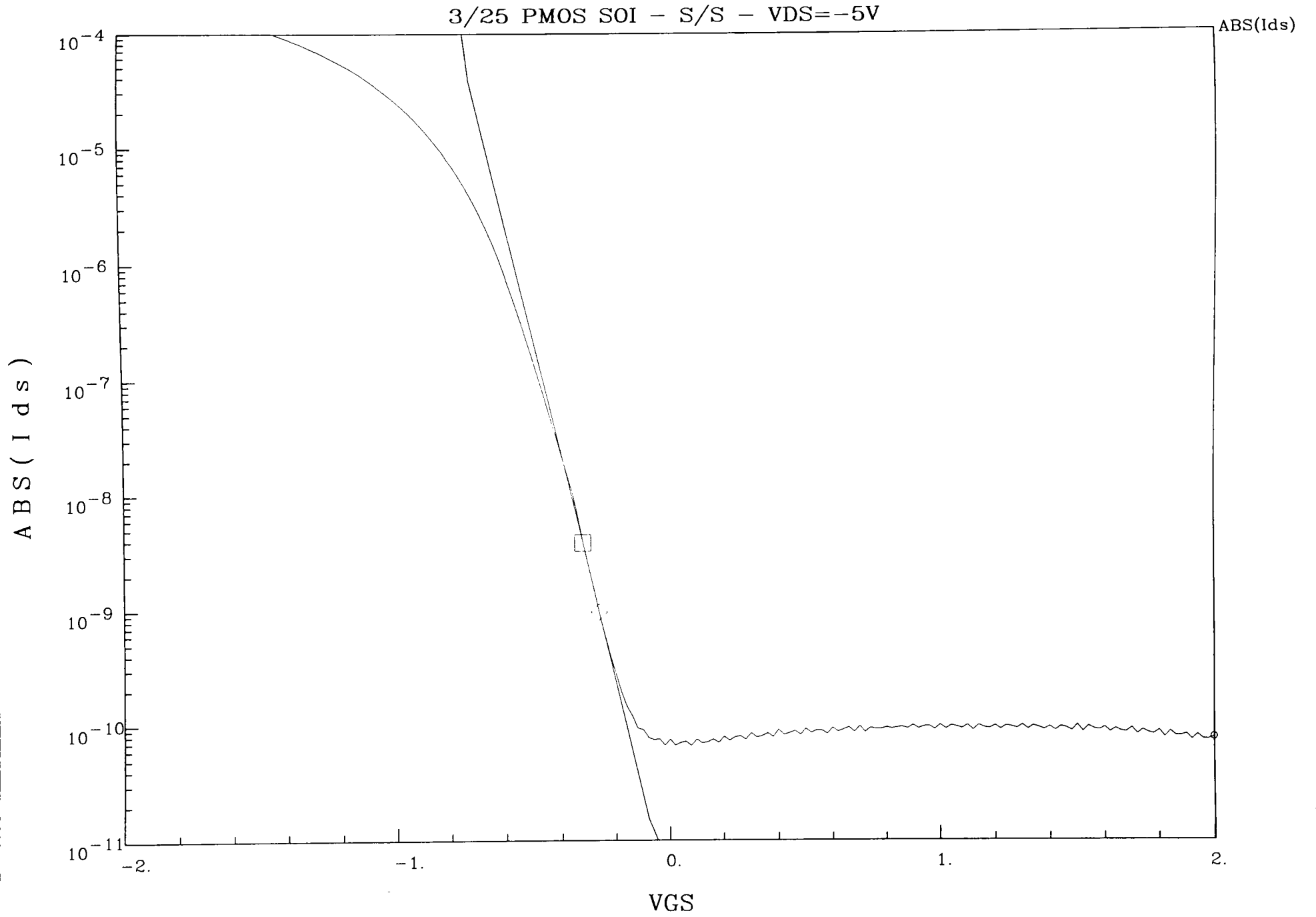
X1: −5.200 Y1: −680.51u Slope: 15.938u
X2: −6.0000 Y2: −693.26u Y−int: −597.63u
DX: 800.00m DY: 12.75u X−int: 37.50



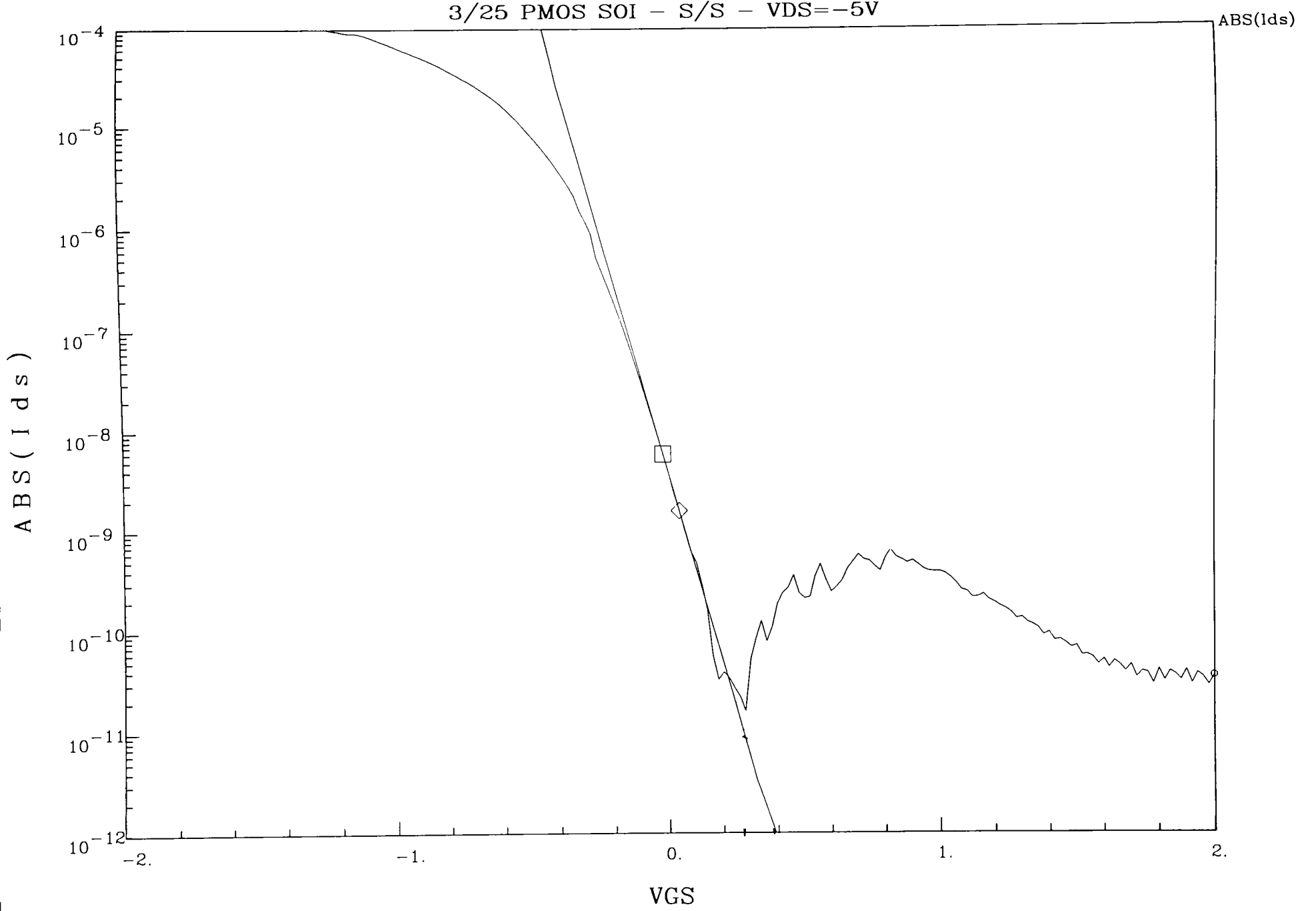
Y1: -513.31u Slope: 12.091u
Y2: -498.80u Y-int: -431.1u
DY: -14.510u X-int: 35.651



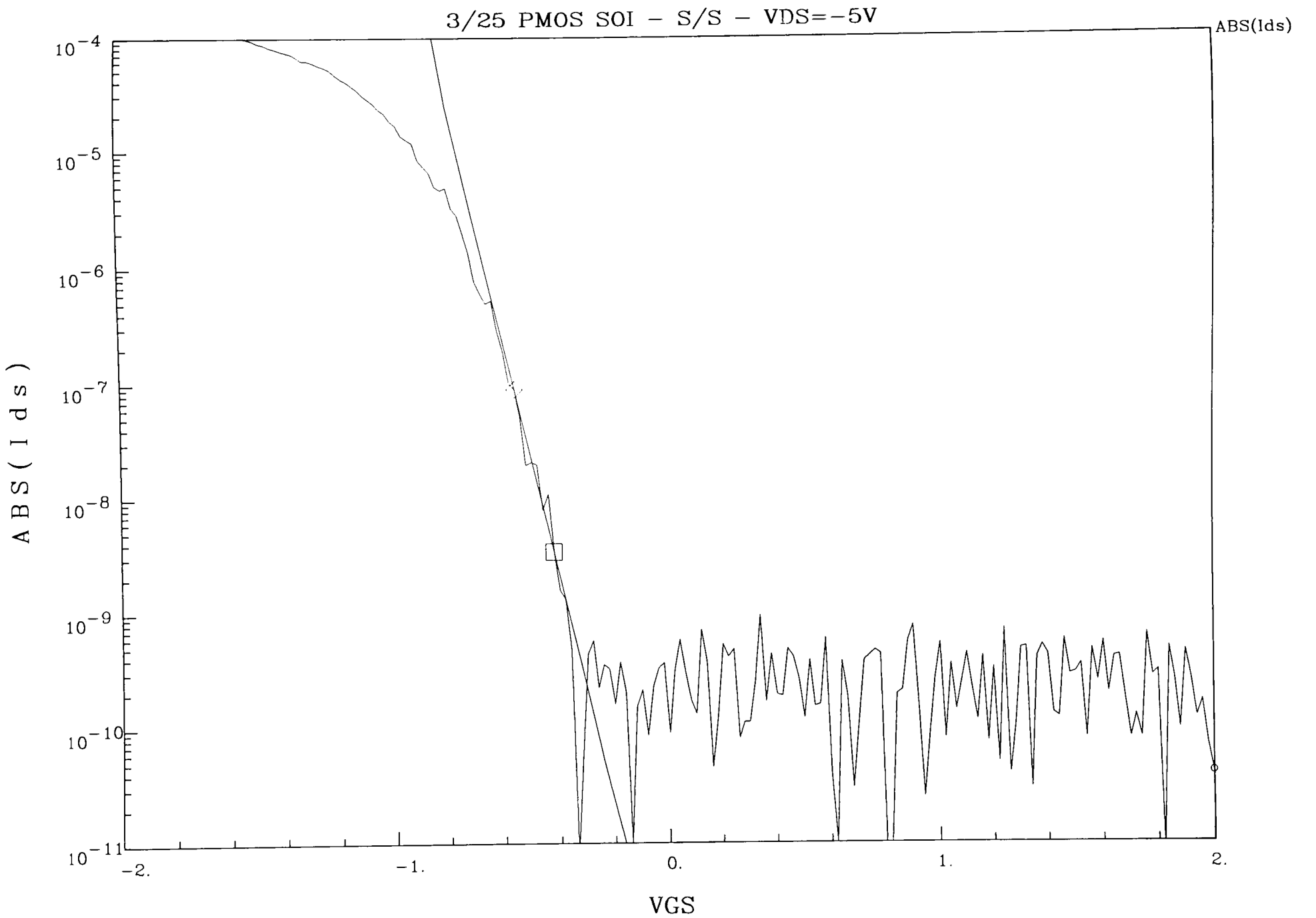
X1: -6.8000
X2: -5.600
DX: -1.2000



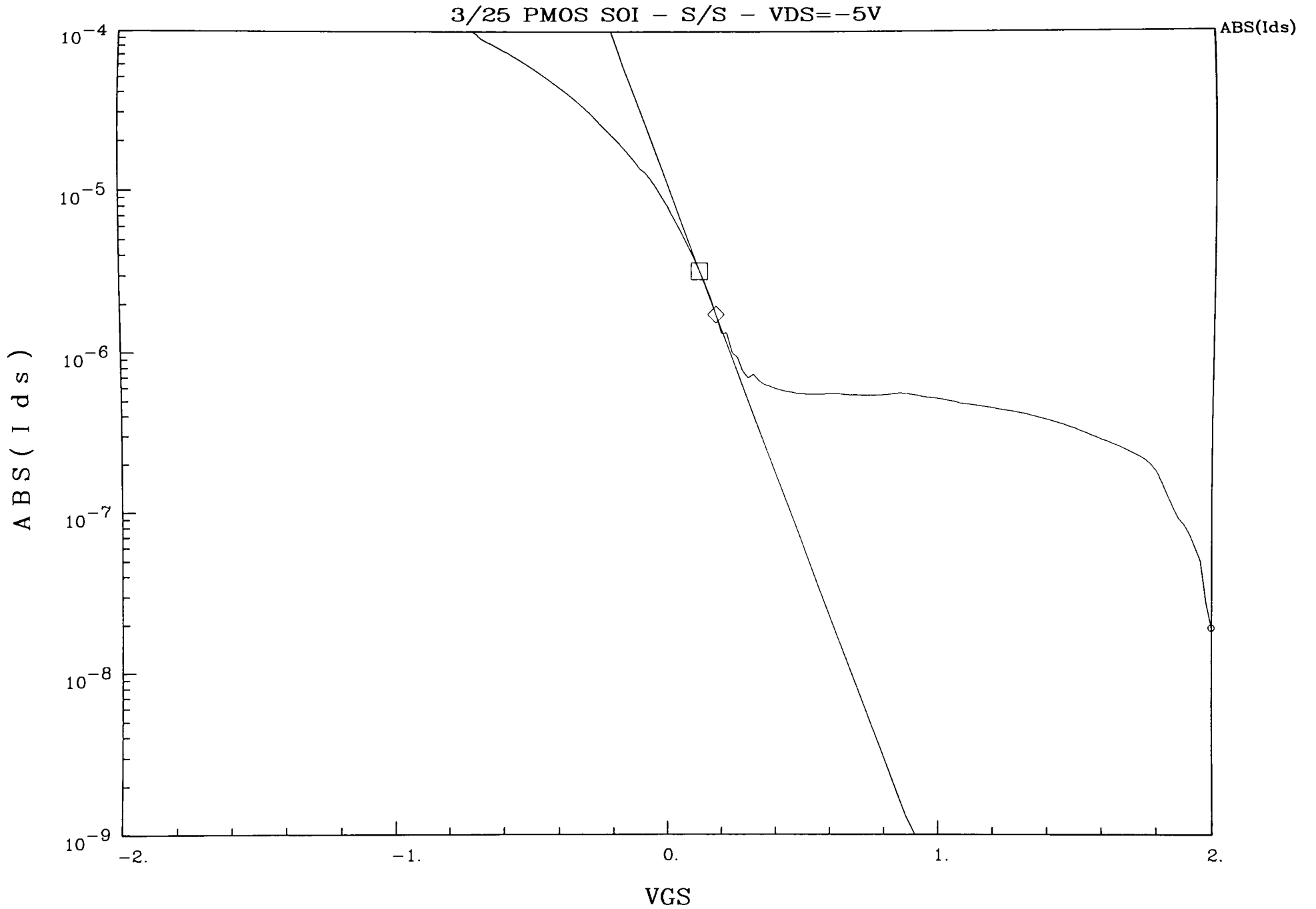
X1: -320.0m Y1: 3.825n A: 2.396p
X2: -260.0m Y2: 959.46p B: -23.05
DX: -60.000m DY: 2.8654n y = A*e~(B*x)



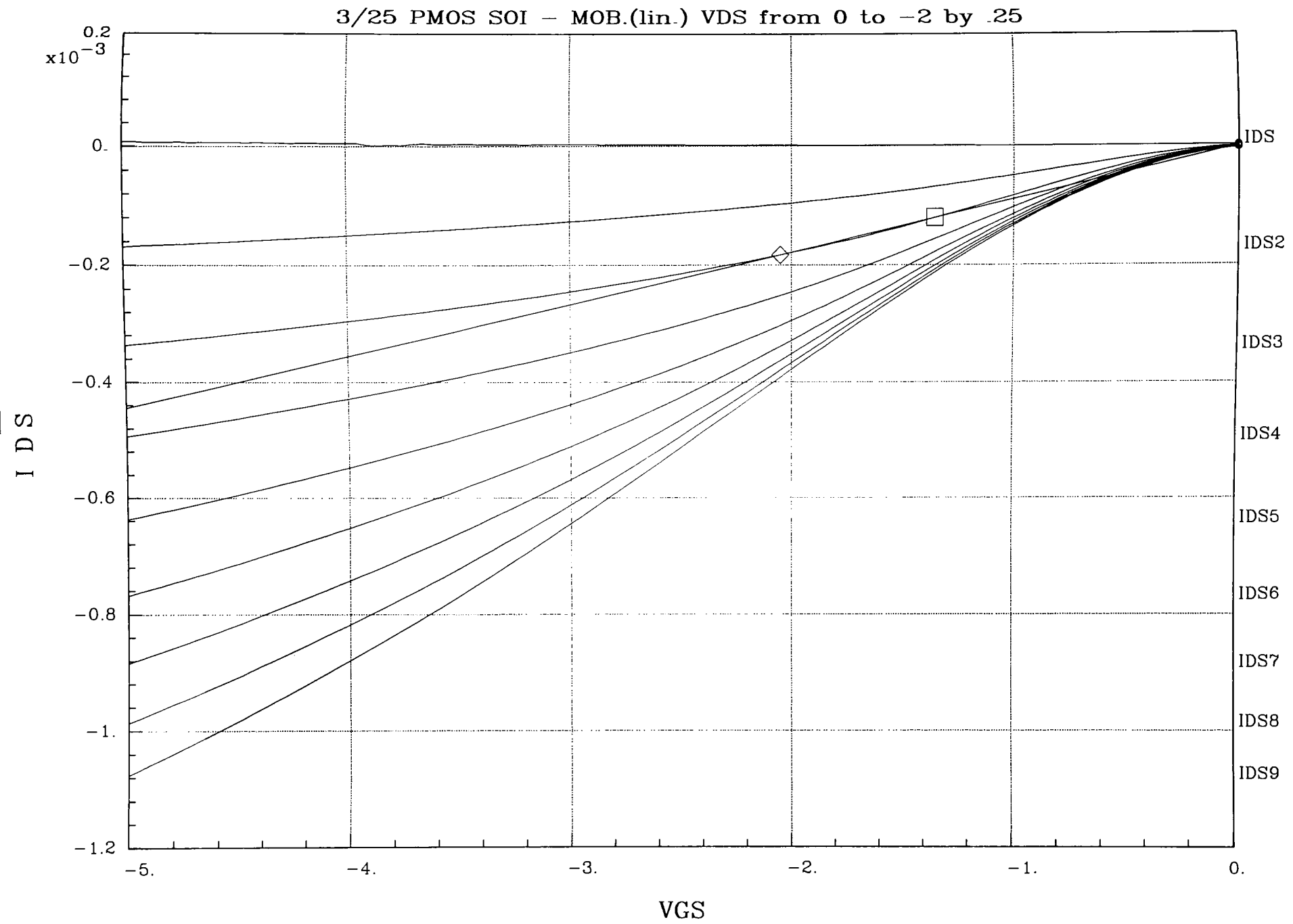
X1: –20.00m Y1: 5.8700n A: 3.7880n
X2: 40.00m Y2: 1.5776n B: –21.900
DX: –60.00m DY: 4.2926n y = A*e~(B*x)



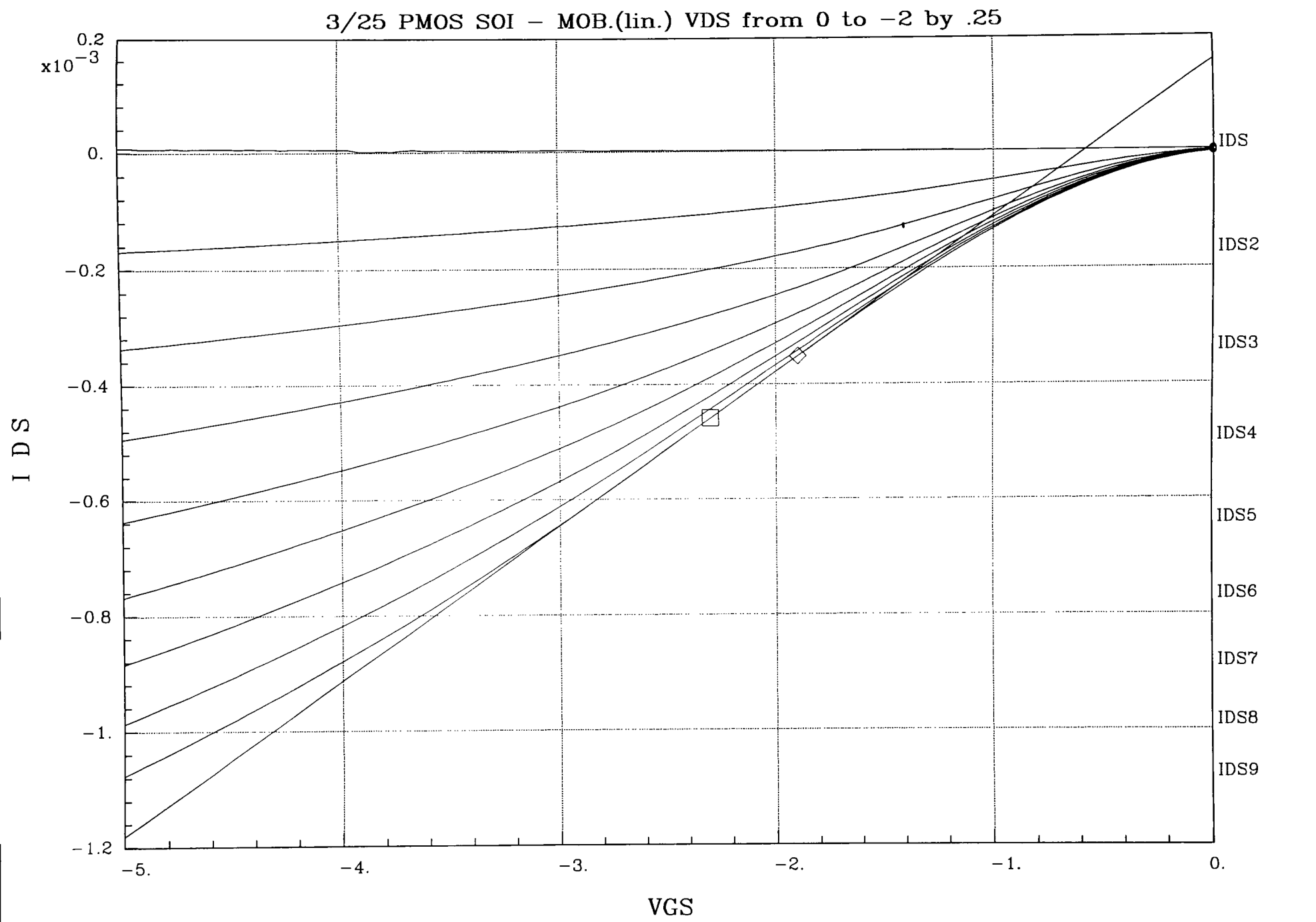
X1: -420.0m Y1: 3.3650n A: 182.50f
X2: -560.00m Y2: 88.898n B: -23.387
DX: 140.00m DY: -85.532n y = A*e~(B*x)



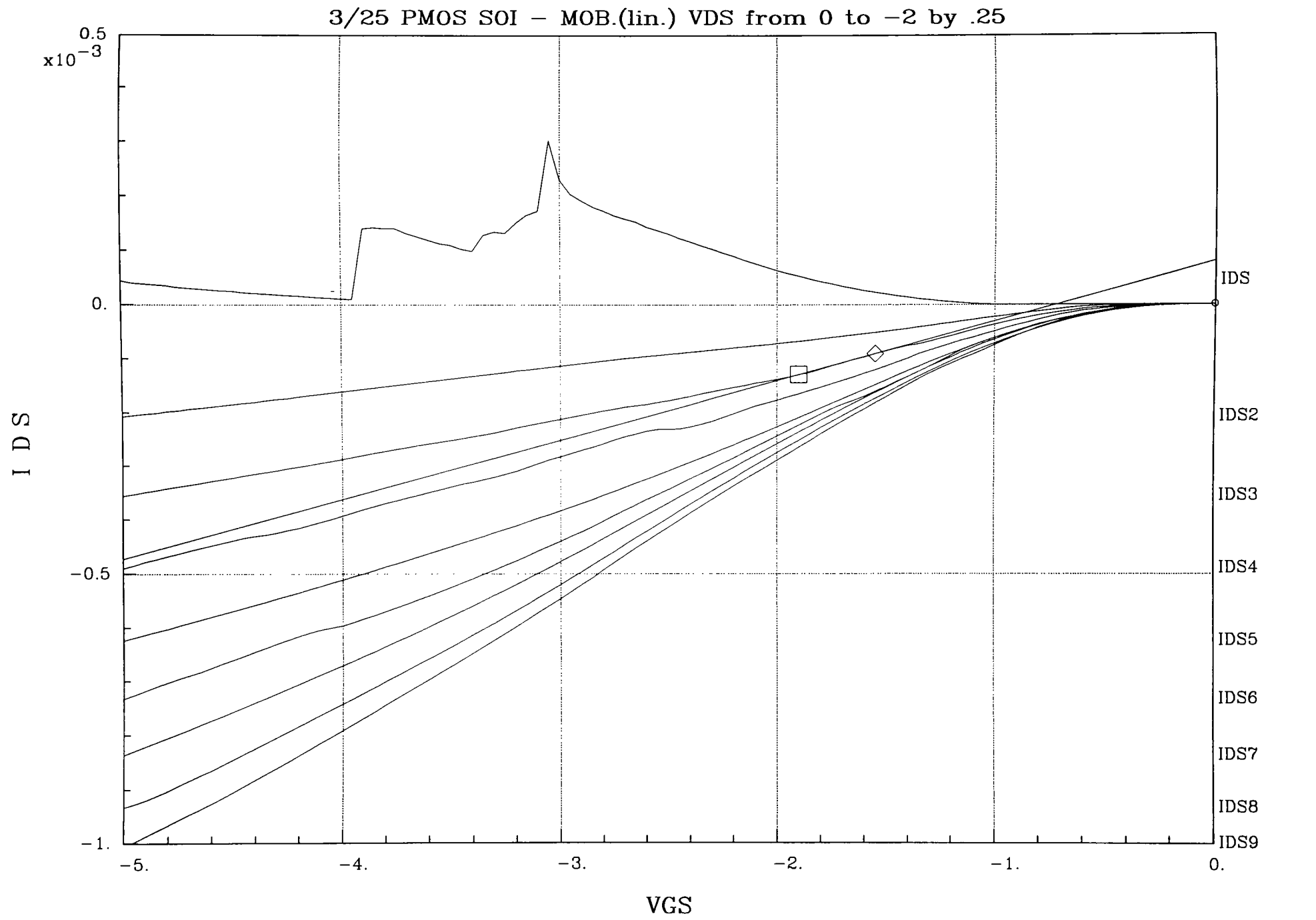
X1: 180.00m Y1: 1.722u A: 10.926u
X2: 120.0m Y2: 3.188u B: −10.264
DX: 60.000m DY: −1.466u y = A*e~(B*x)



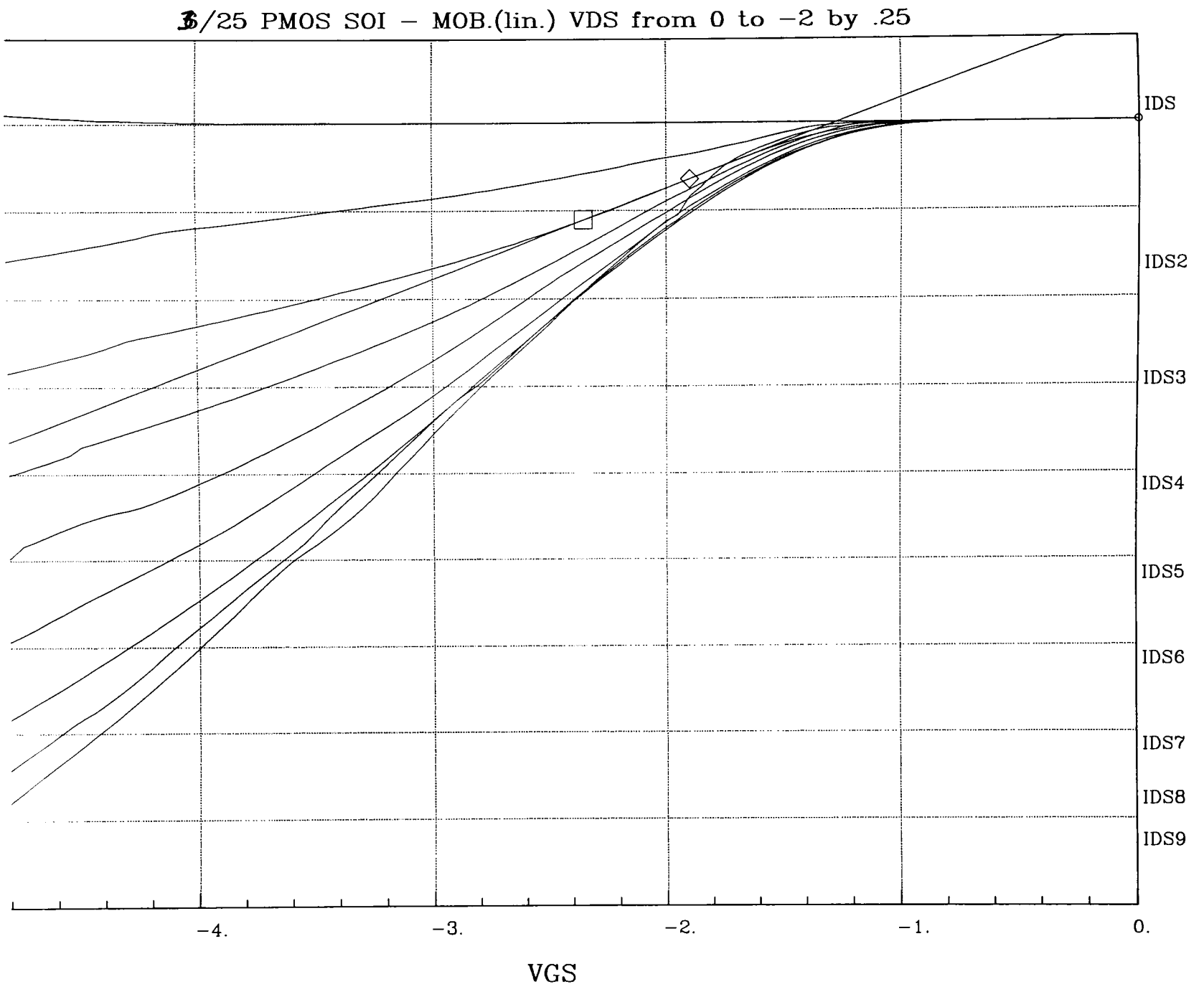
X1: −1.3500 Y1: −120.94u Slope: 88.714u
X2: −2.050 Y2: −183.04u Y−int: −1.1857u
DX: 700.0m DY: 62.10u X−int: 13.366m



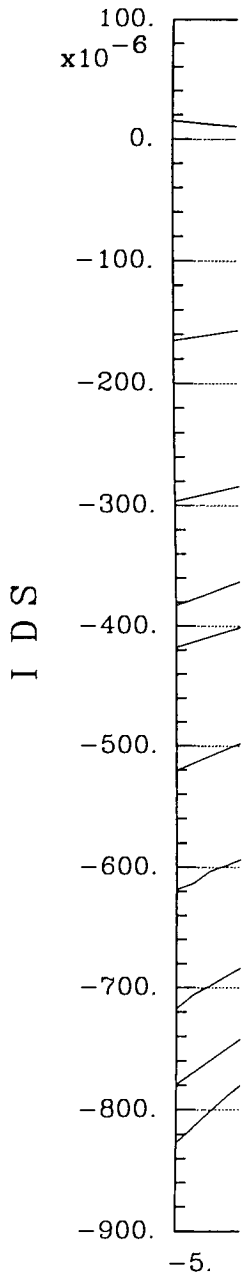
X1: −1.900 Y1: −352.06u Slope: 267.36u
X2: −2.300 Y2: −459.00u Y−int: 155.90u
DX: 400.0m DY: 106.94u X−int: −583.14m



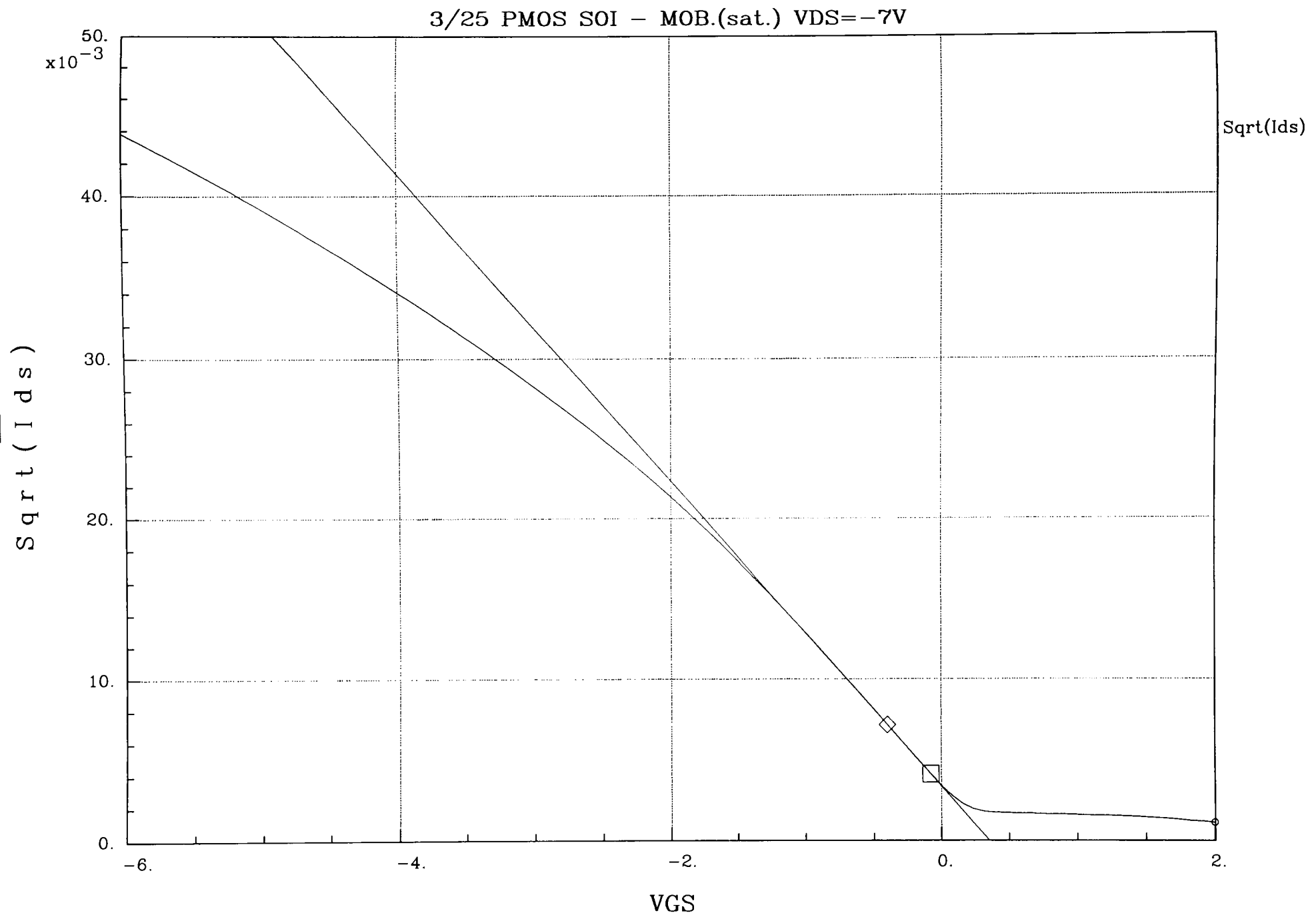
X1: −1.900 Y1: −130.06u Slope: 110.64u
X2: −1.550 Y2: −91.324u Y−int: 80.171u
DX: −350.00m DY: −38.726u X−int: −724.6m



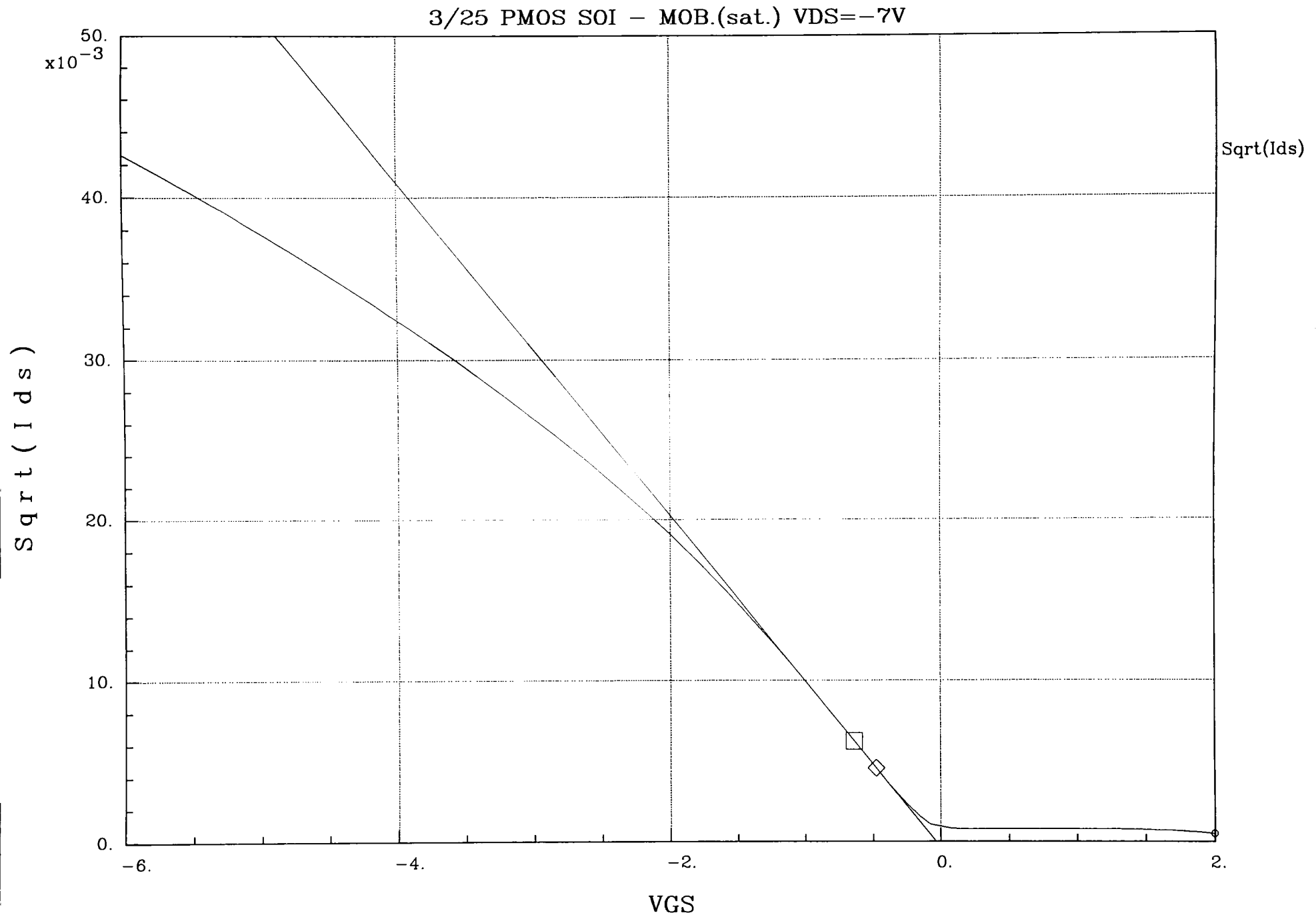
Y1: −64.497u Slope: 102.8u
Y2: −110.74u Y−int: 130.8u
DY: 46.253u X−int: −1.2726



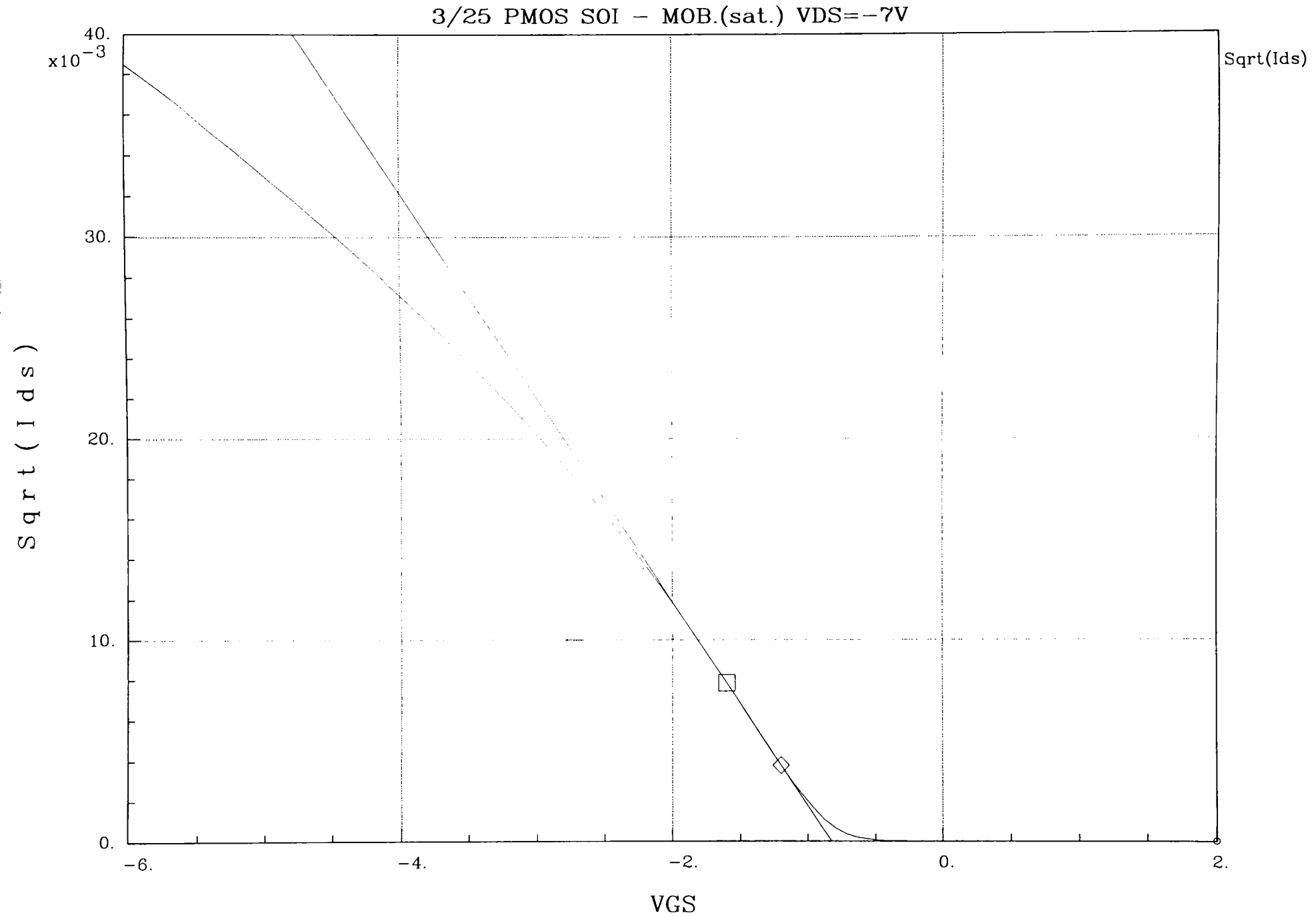
X1: −1.900
X2: −2.350
DX: 450.0m



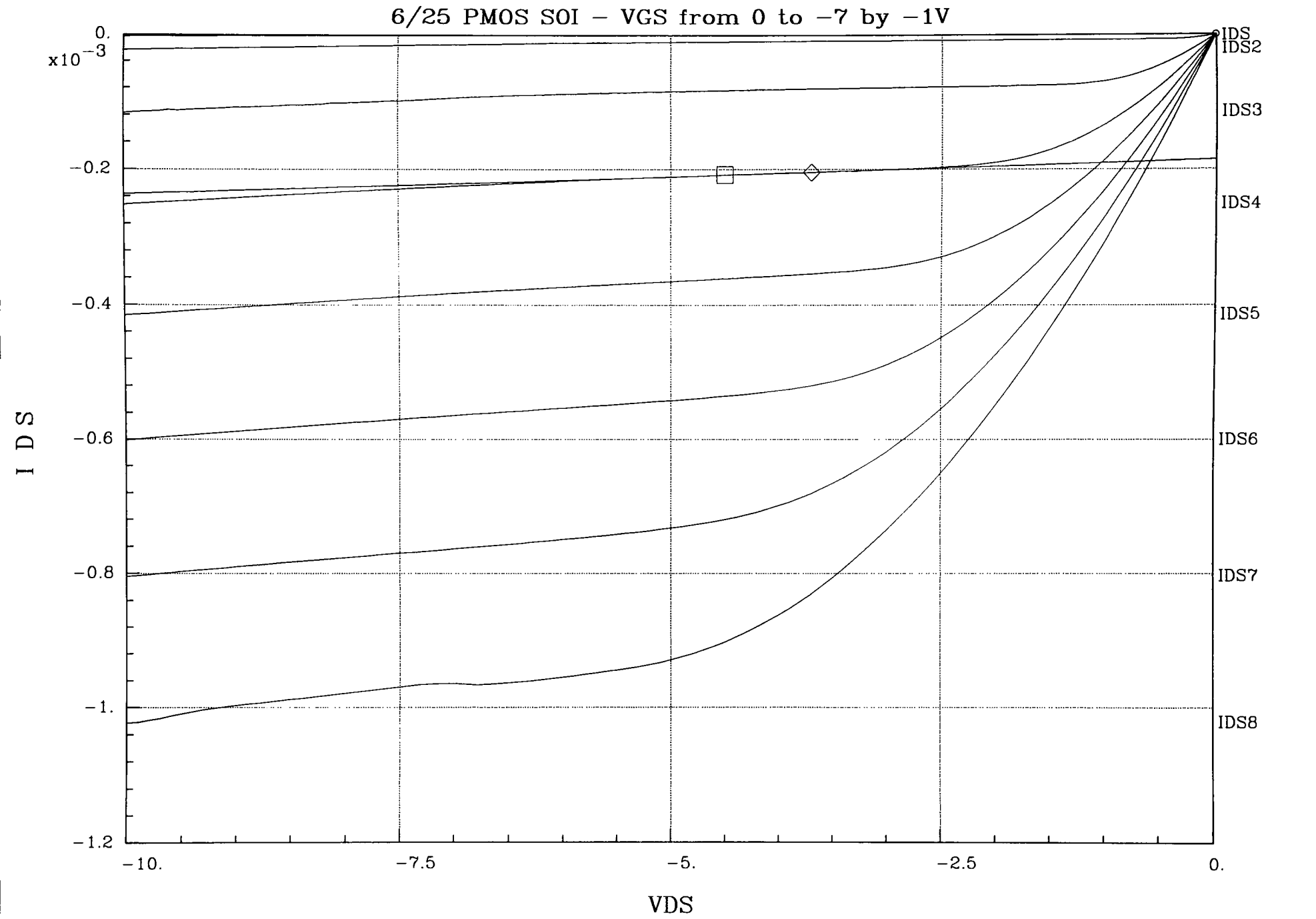
X1: −400.00m Y1: 7.1361m Slope: −9.5071m
X2: −80.00m Y2: 4.094m Y−int: 3.3333m
DX: −320.00m DY: 3.0422m X−int: 350.61m



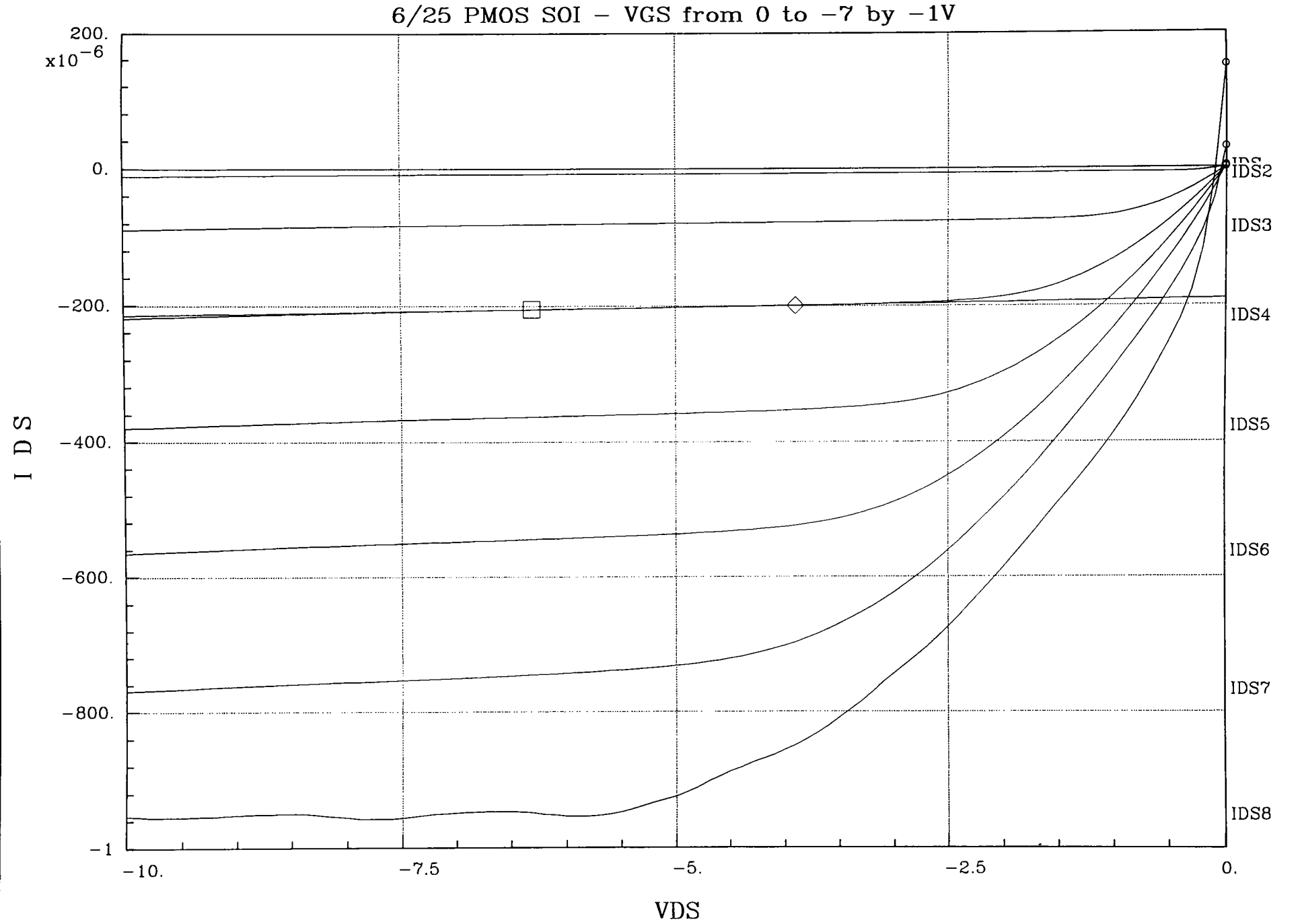
X1: −640.0m Y1: 6.207m Slope: −10.327m
X2: −480.0m Y2: 4.5547m Y−int: −401.9u
DX: −160.0m DY: 1.6521m X−int: −38.92m



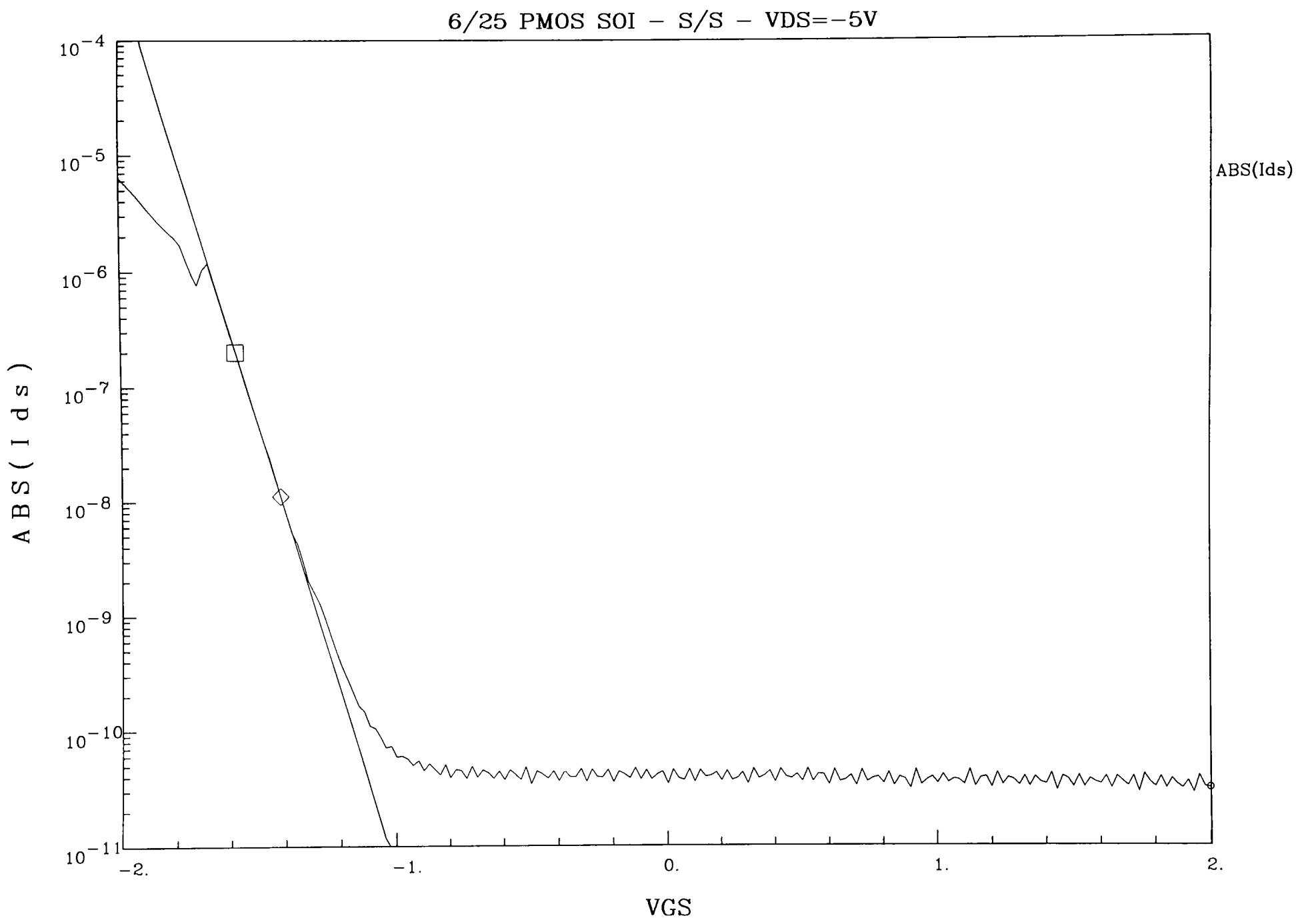
X1: -1.6000 Y1: 7.8118m Slope: -10.146m
X2: -1.2000 Y2: 3.7537m Y-int: -8.4207m
DX: -400.0m DY: 4.0581m X-int: -830.00m



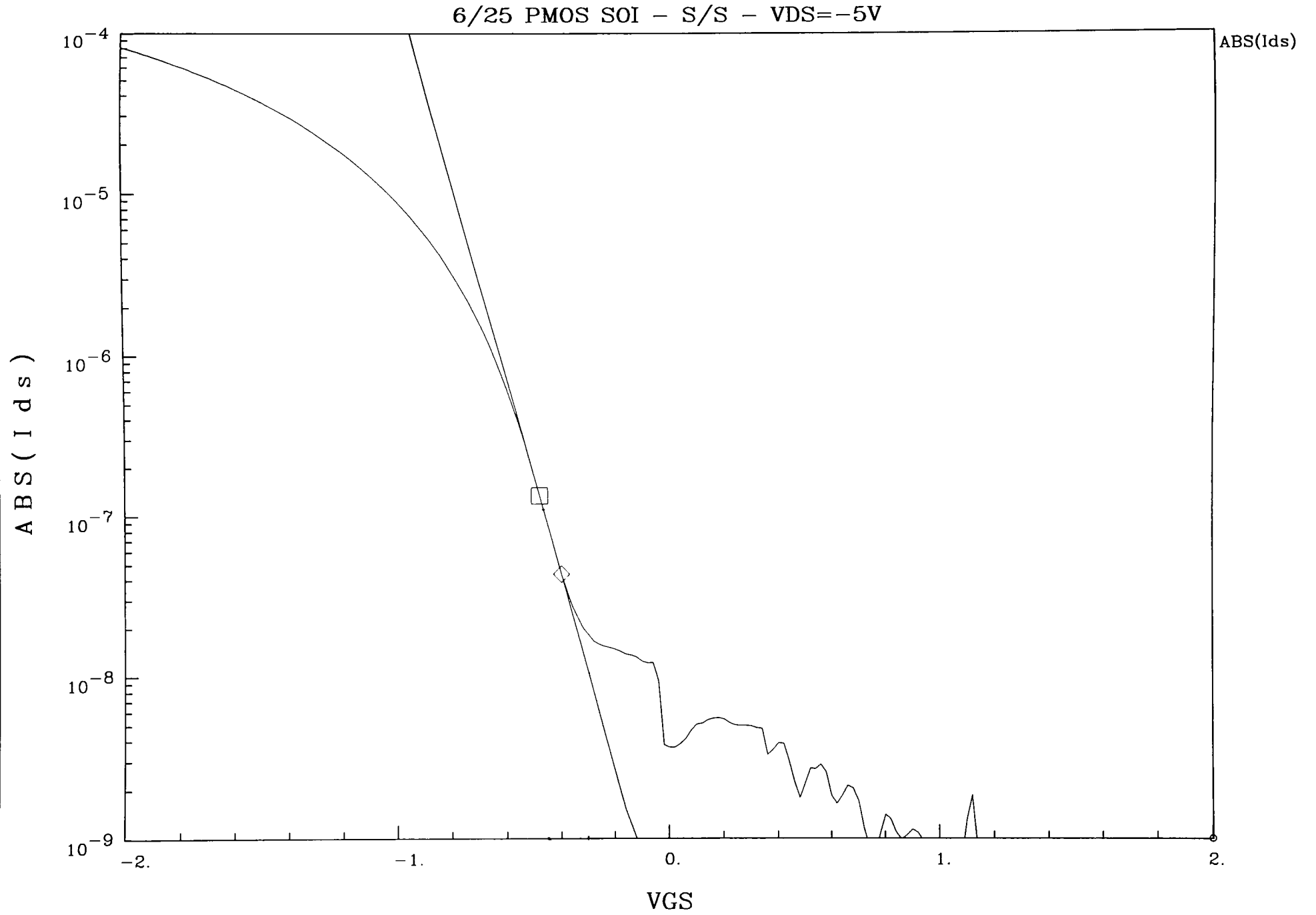
X1: −4.5000 Y1: −208.90u Slope: 5.0626u
X2: −3.7000 Y2: −204.86u Y−int: −186.11u
DX: −800.0m DY: −4.0500u X−int: 36.764



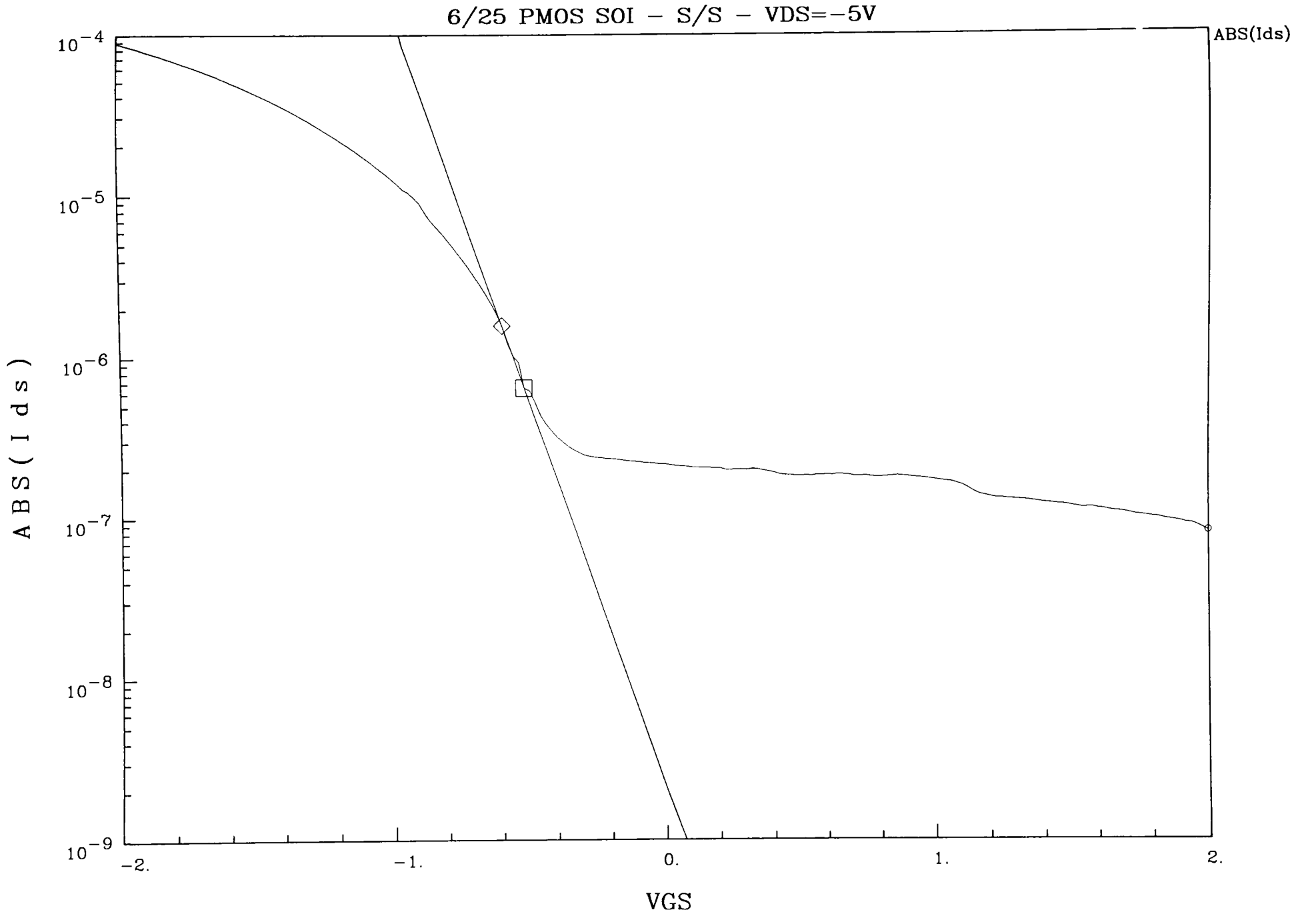
X1: −3.9000 Y1: −199.74u Slope: 2.4376u
X2: −6.3000 Y2: −205.6u Y−int: −190.24u
DX: 2.4000 DY: 5.8500u X−int: 78.05



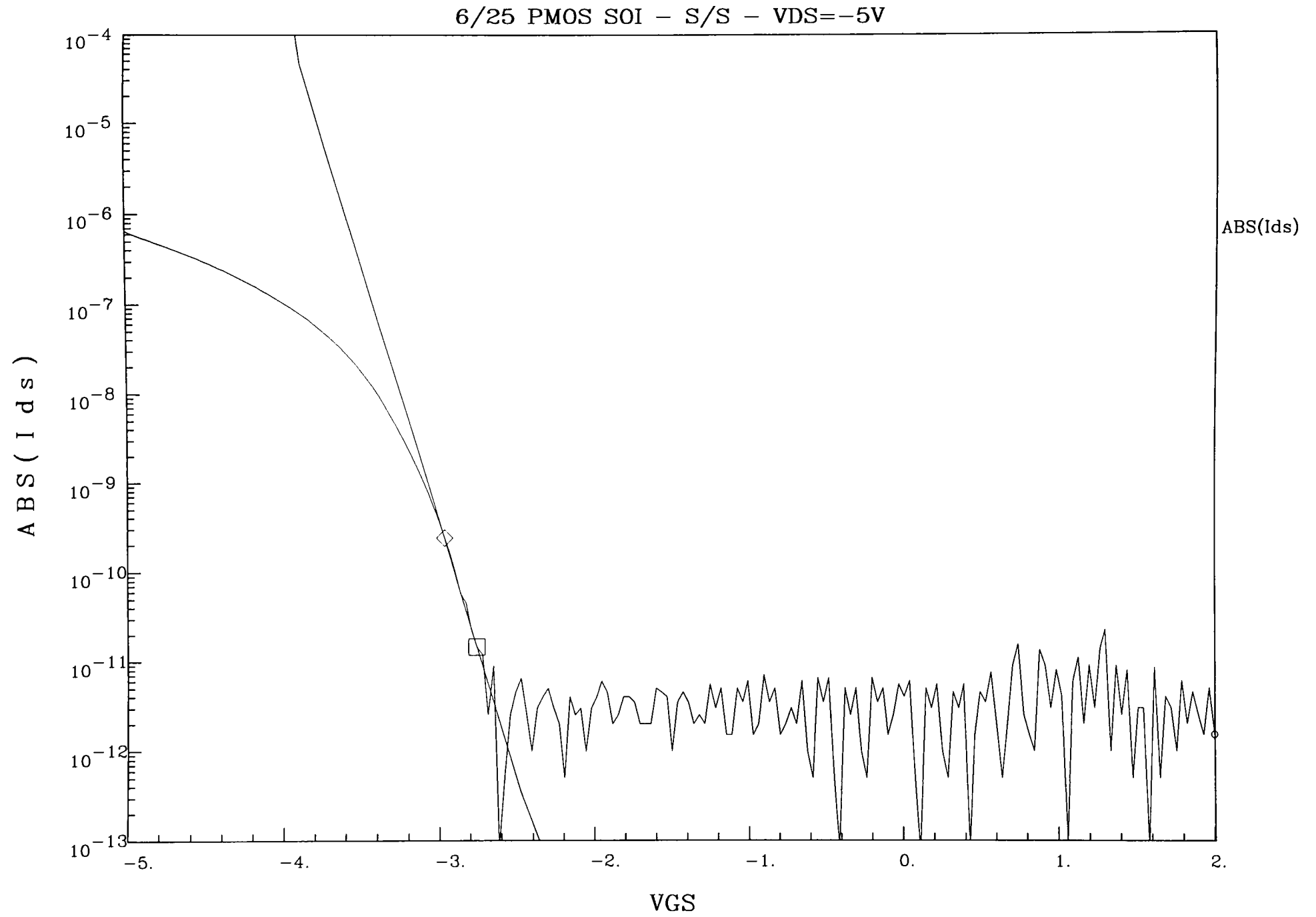
X1: –1.420 Y1: 11.134n A: 84.15
X2: –1.5800 Y2: 199.44n B: –18.034
DX: 160.00m DY: –188.31n y = A*e~(B*x)



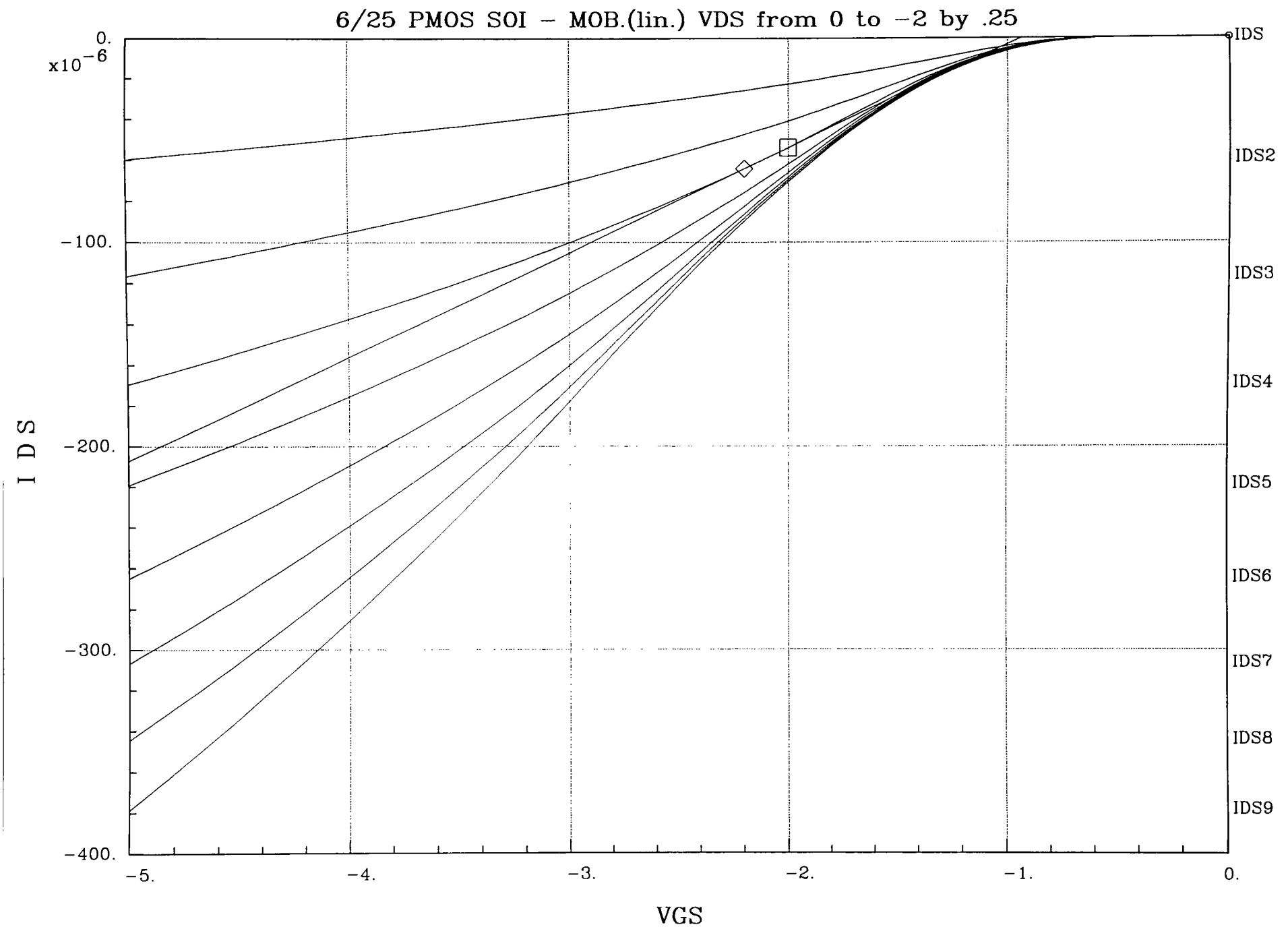
X1: −480.0m Y1: 133.80n A: 160.17p
X2: −400.00m Y2: 43.60n B: −14.017
DX: −80.00m DY: 90.200n y = A*e~(B*x)



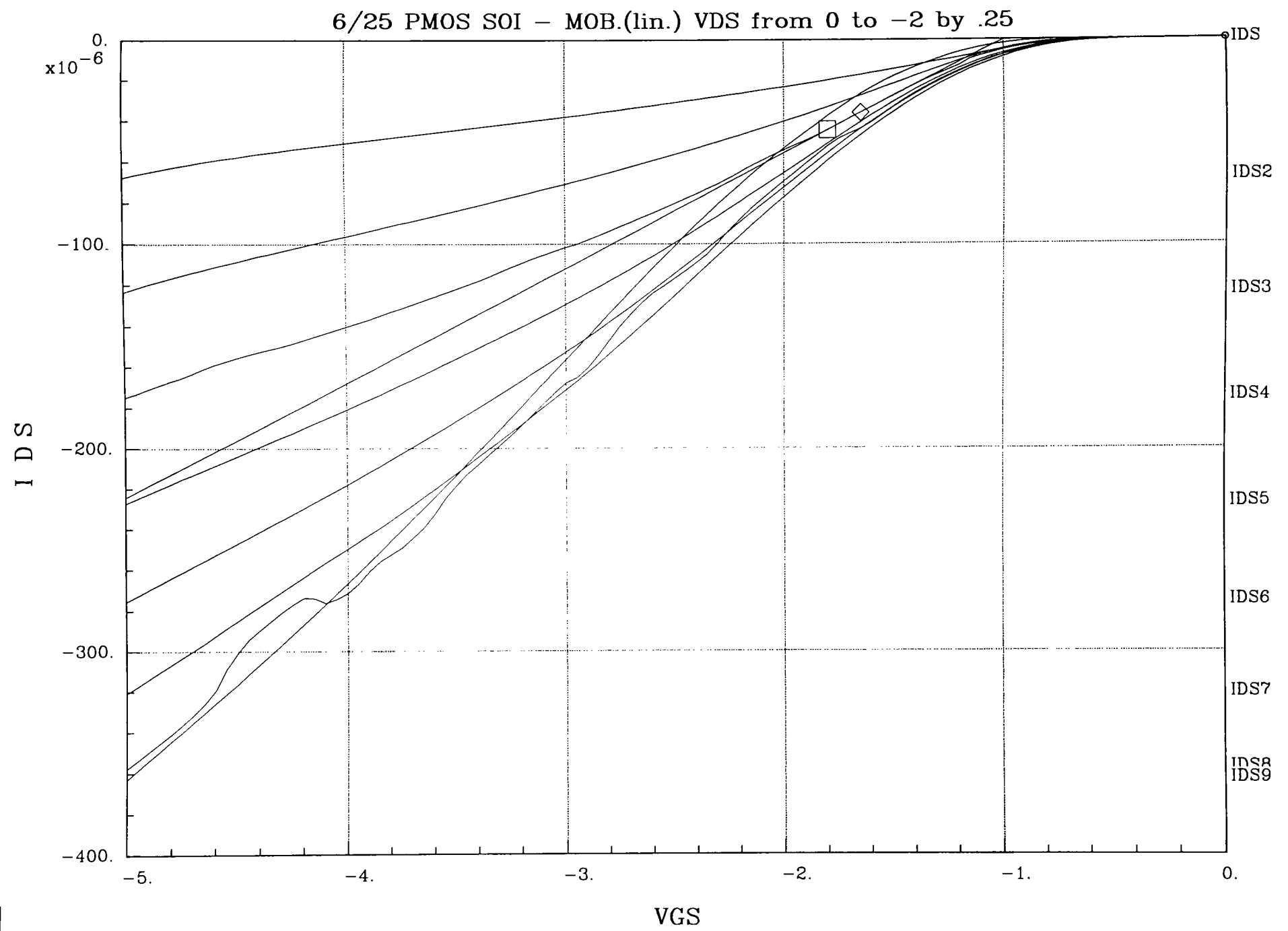
X1: −520.0m Y1: 651.0n A: 2.0233n
X2: −600.00m Y2: 1.5824u B: −11.103
DX: 80.000m DY: −931.50n y = A*e~(B*x)



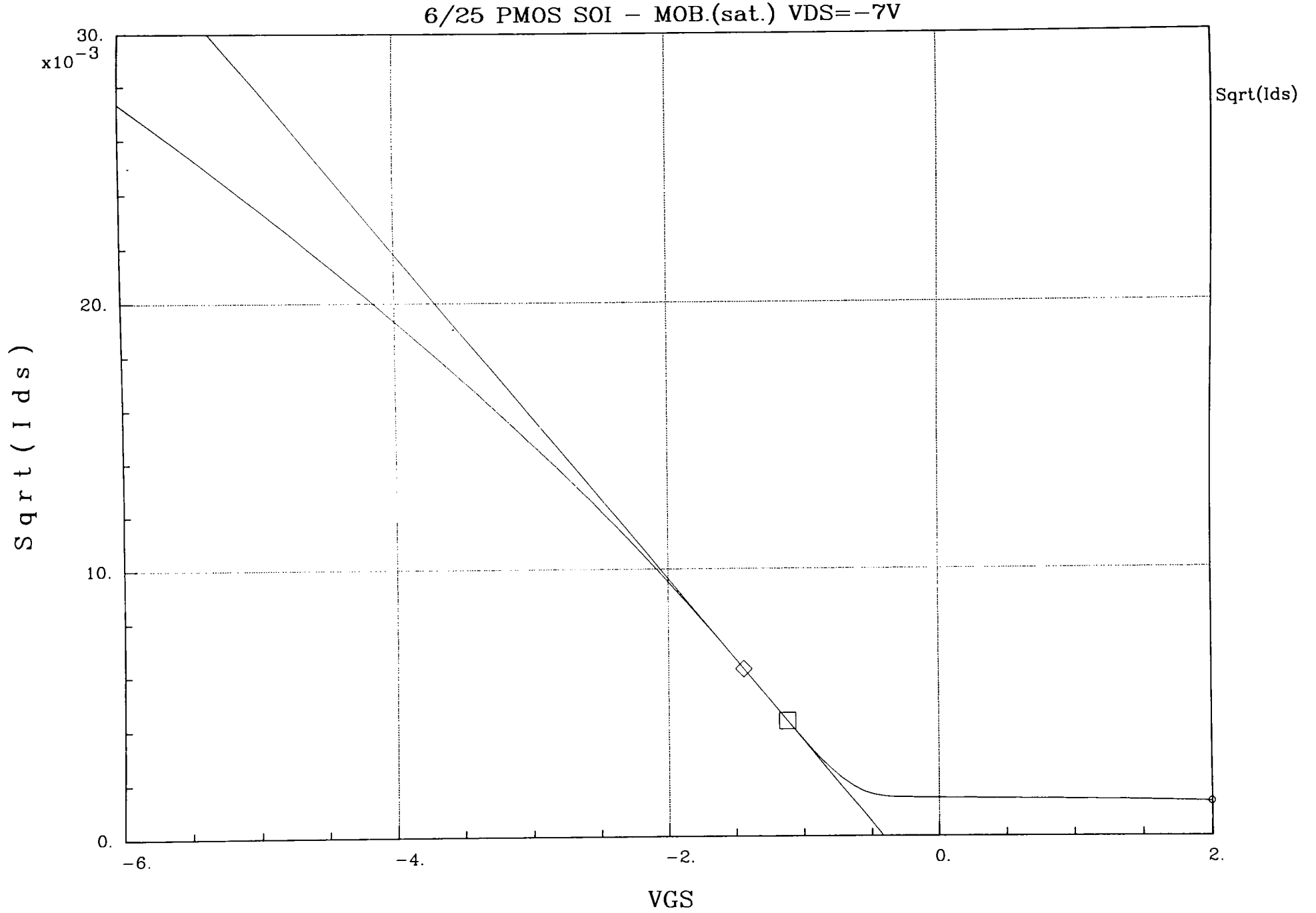
X1: −2.9700 Y1: 240.0p A: 1.3870
X2: −2.760 Y2: 14.50p B: −13.364
DX: −210.00m DY: 225.5p y = A*e~(B*x)



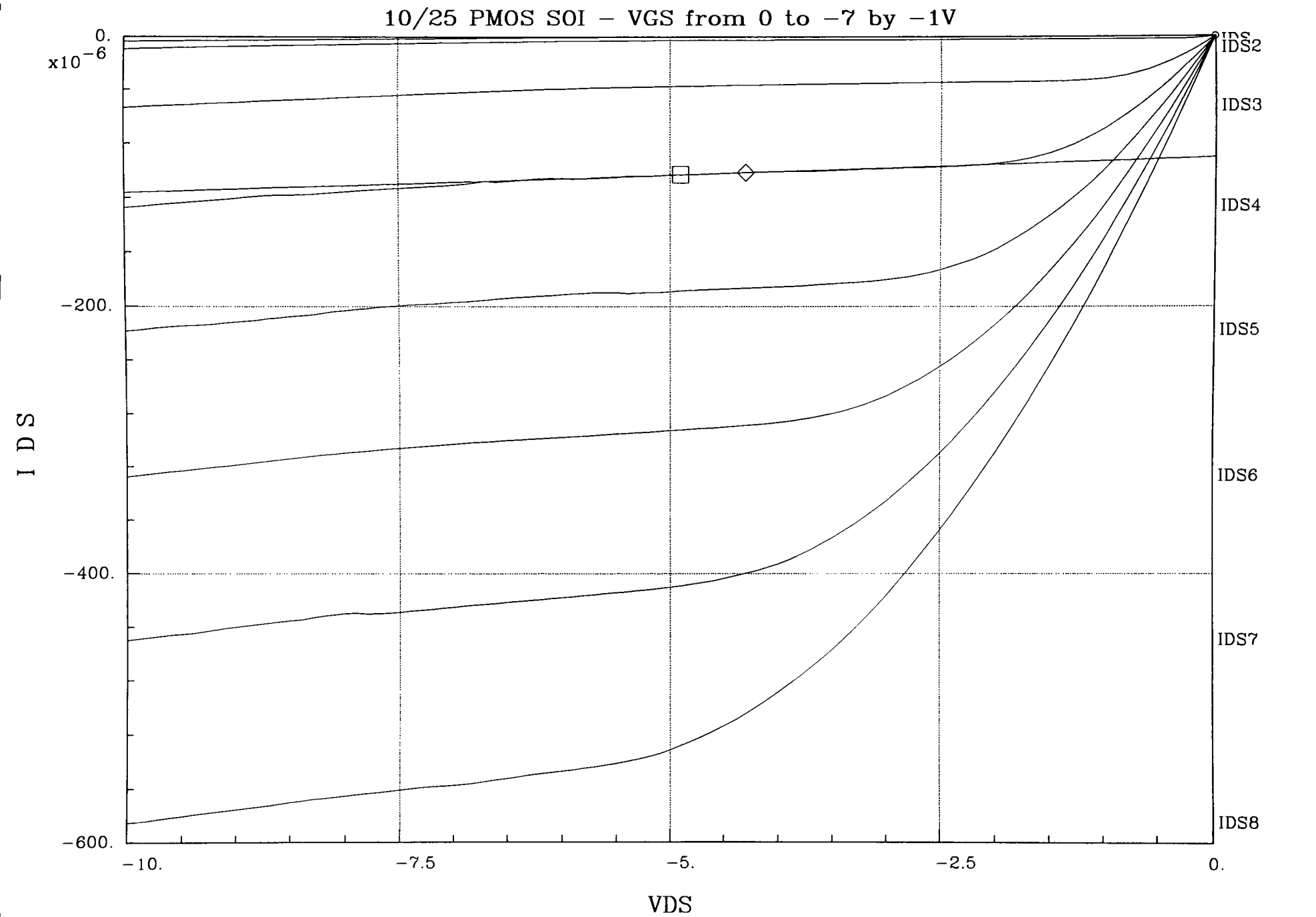
X1: −2.2000 Y1: −64.384u Slope: 51.044u
X2: −2.0000 Y2: −54.176u Y−int: 47.914u
DX: −200.00m DY: −10.21u X−int: −938.7m



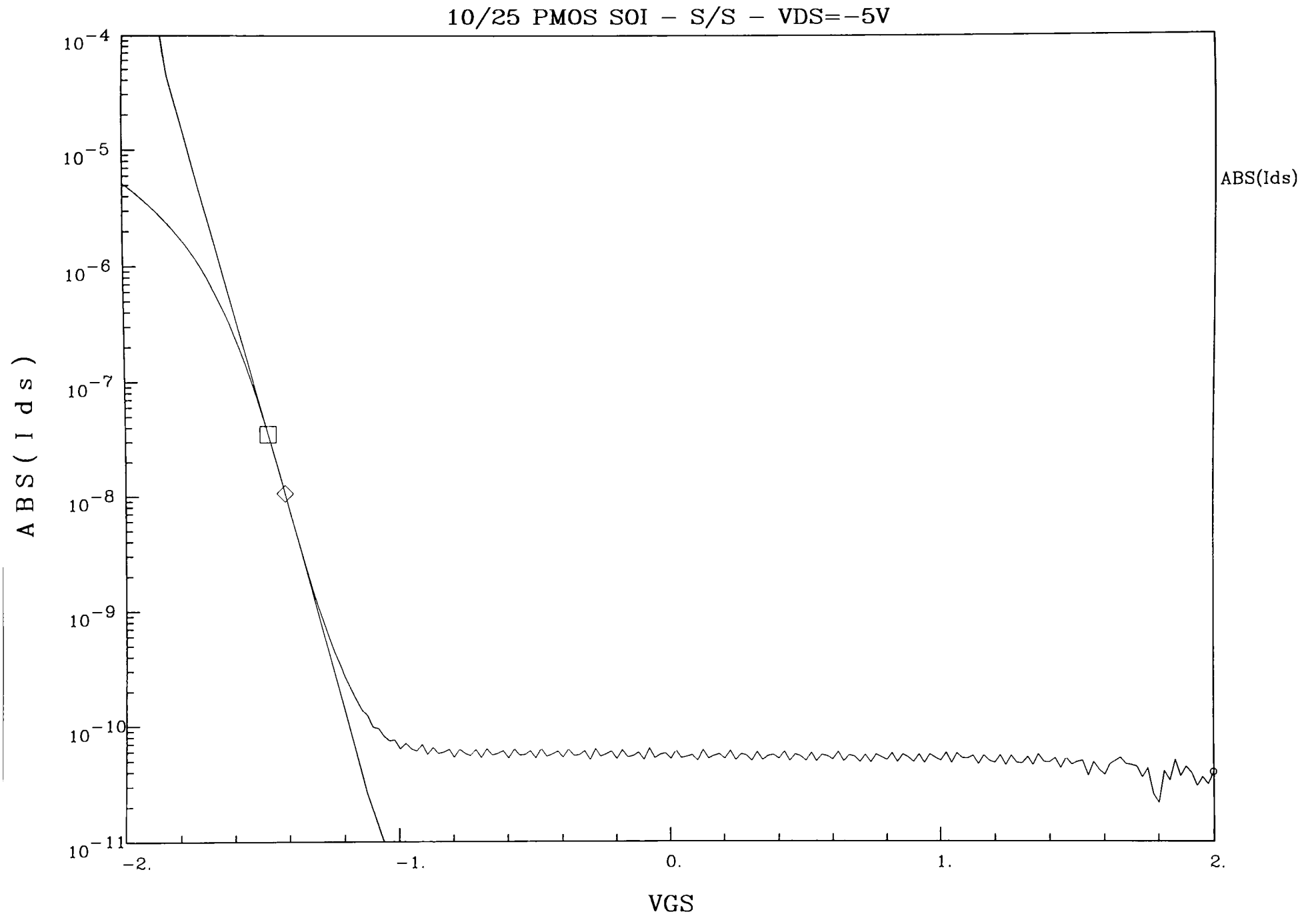
X1: −1.800 Y1: −44.963u Slope: 56.027u
X2: −1.650 Y2: −36.56u Y−int: 55.884u
DX: −150.0m DY: −8.4040u X−int: −997.46m



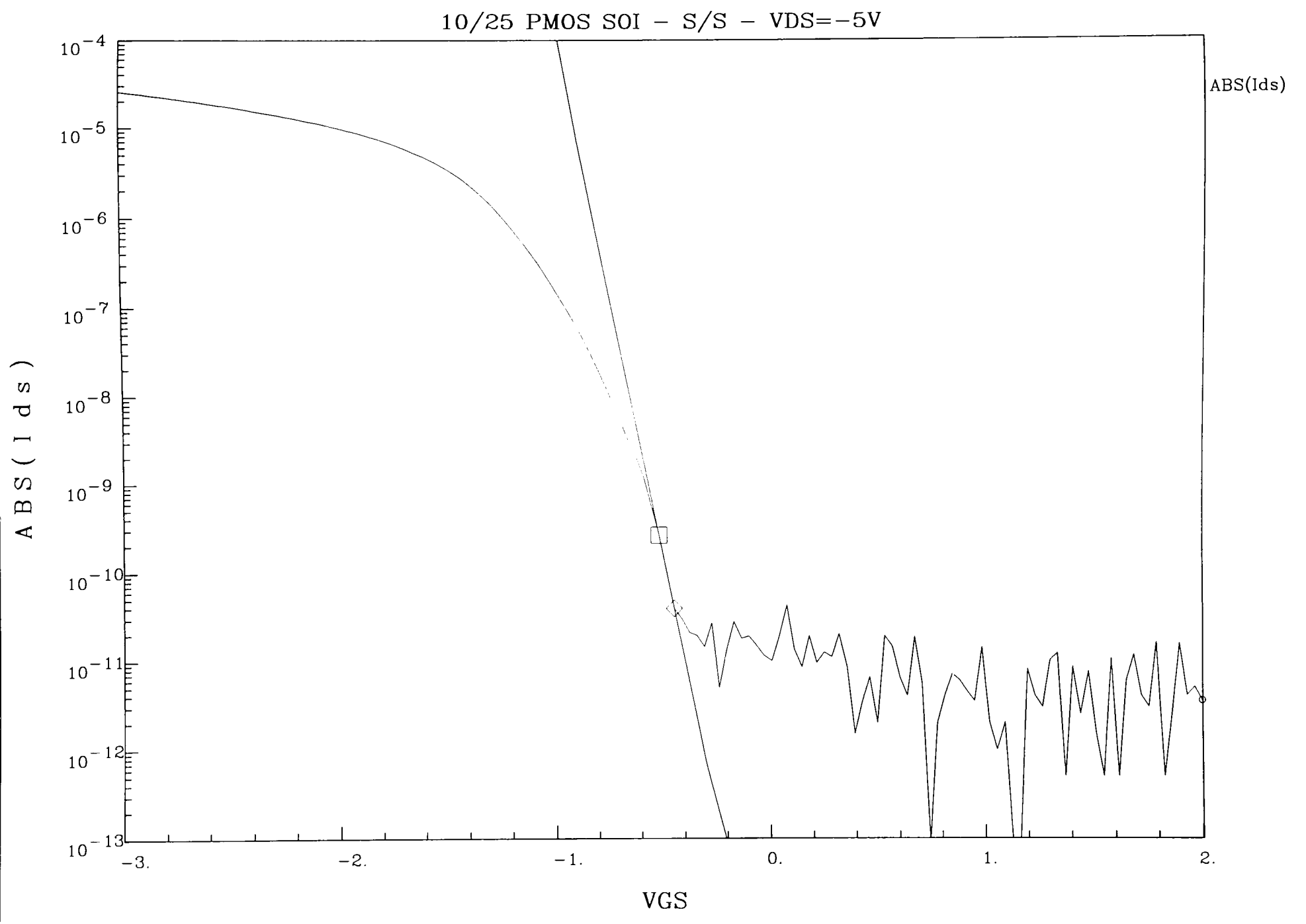
X1: –1.4400 Y1: 6.2206m Slope: –6.091m
X2: –1.1200 Y2: 4.2714m Y–int: –2.5504m
DX: –320.00m DY: 1.9491m X–int: –418.73m



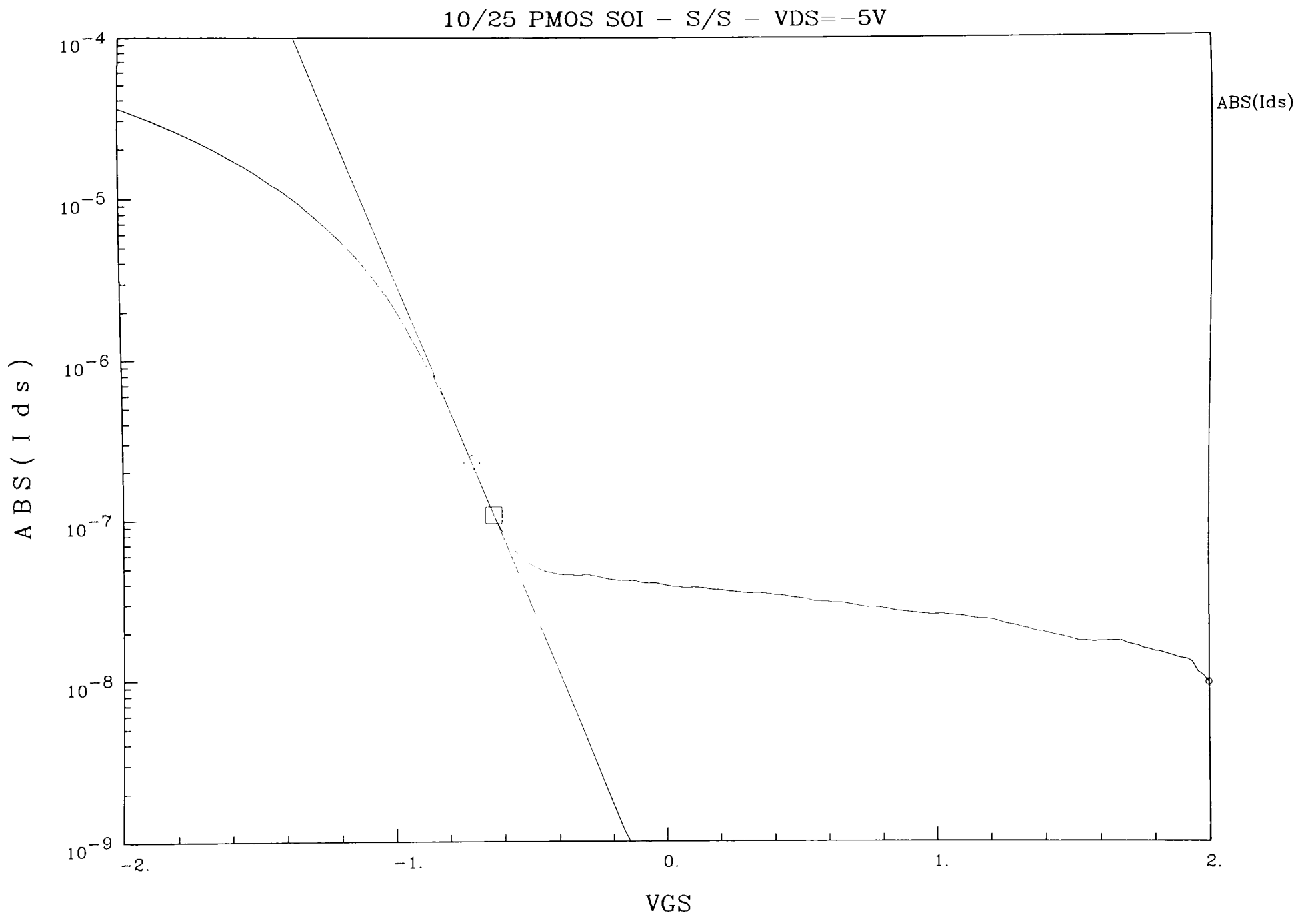
X1: −4.9000 Y1: −103.14u Slope: 2.5833u
X2: −4.3000 Y2: −101.60u Y−int: −90.491u
DX: −600.0m DY: −1.550u X−int: 35.03



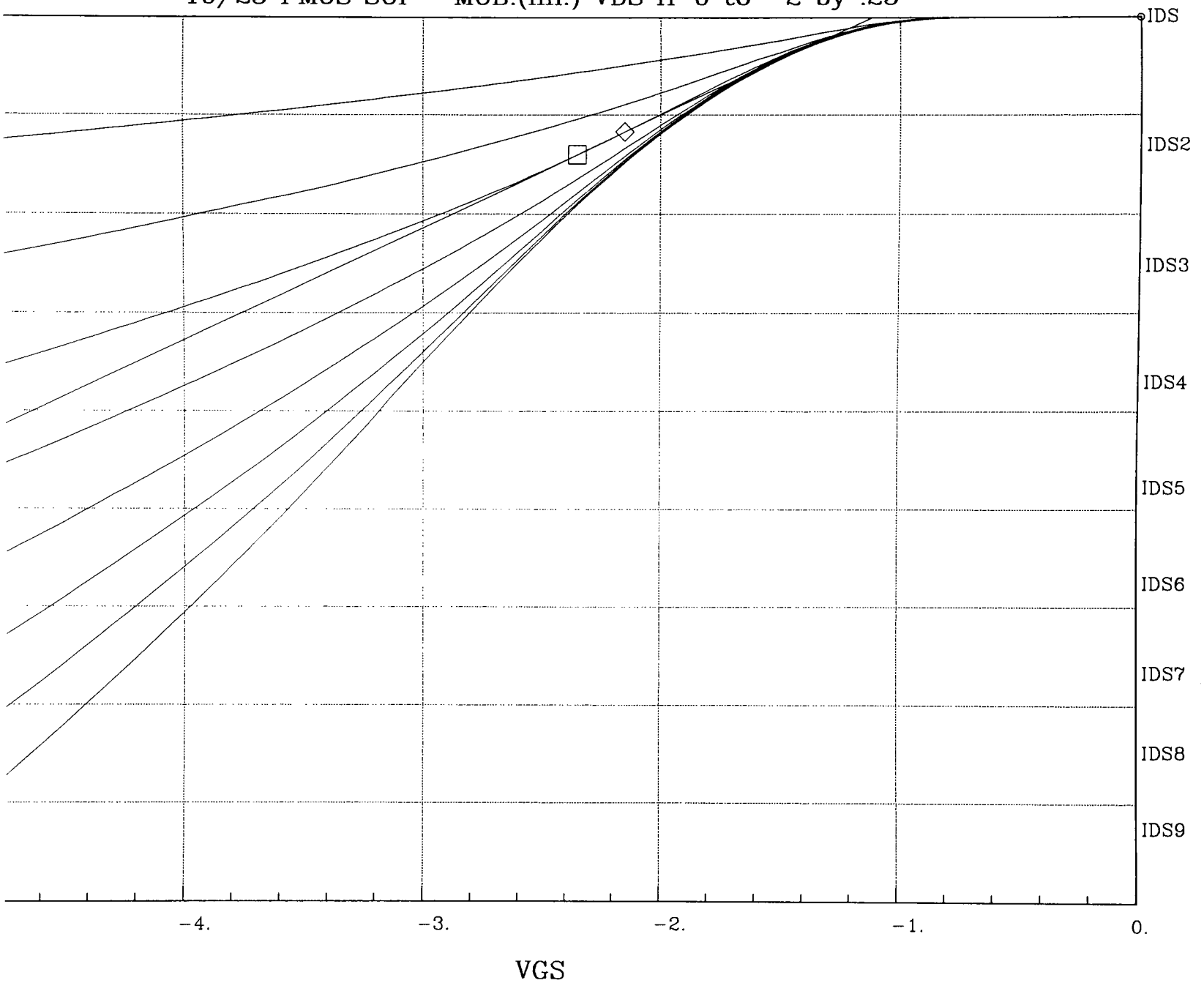
X1: –1.420 Y1: 10.526n A: 5.4168
X2: –1.4800 Y2: 34.79n B: –19.927
DX: 60.000m DY: –24.264n y = A*e~(B*x)



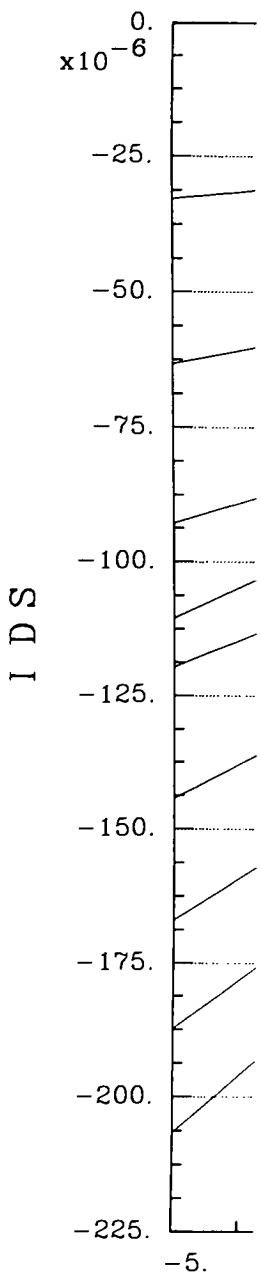
X1: -520.0m Y1: 263.00p A: 201.13a
X2: -450.0m Y2: 39.50p B: -27.083
DX: -70.00m DY: 223.50p y = A*e~(B*x)



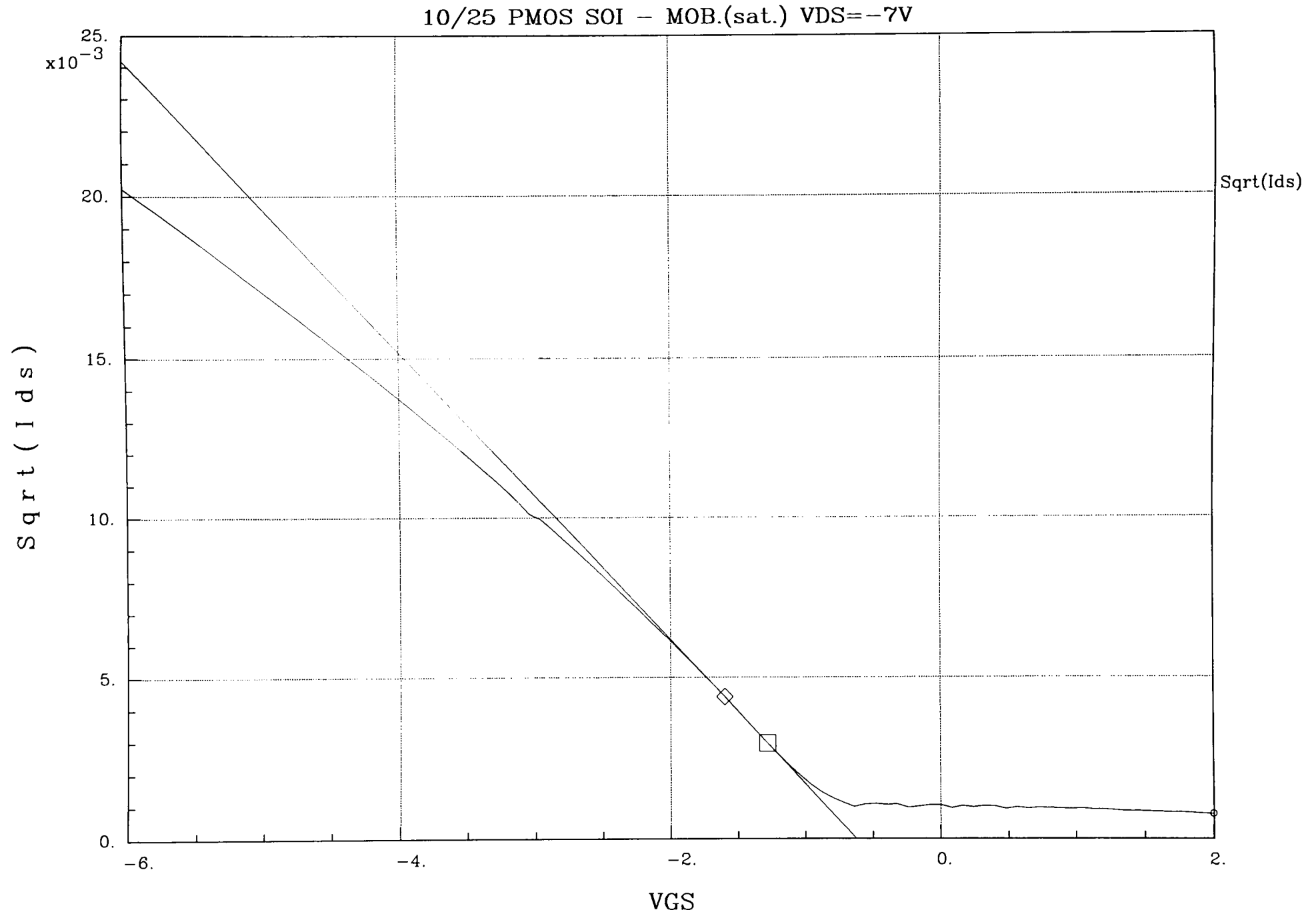
X1: –720.00m Y1: 227.7n A: 255.6p
X2: –640.0m Y2: 107.04n B: –9.4337
DX: –80.000m DY: 120.63n y = A*e~(B*x)



1: −35.06u Slope: 28.450u
2: −29.37u Y−int: 31.80u
Y: −5.6900u X−int: −1.1177



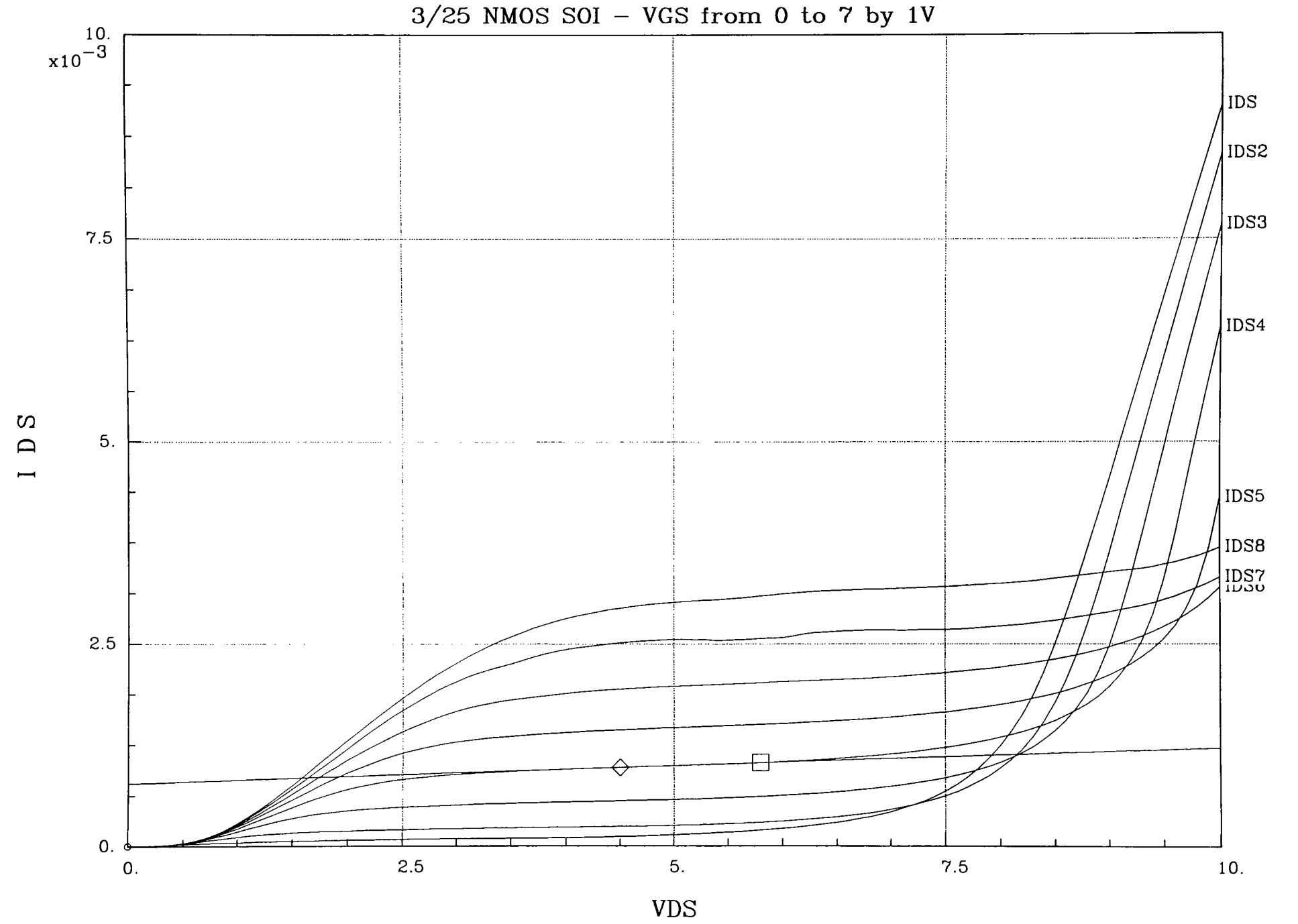
X1: −2.350 Y
X2: −2.1500 Y
DX: −200.0m D



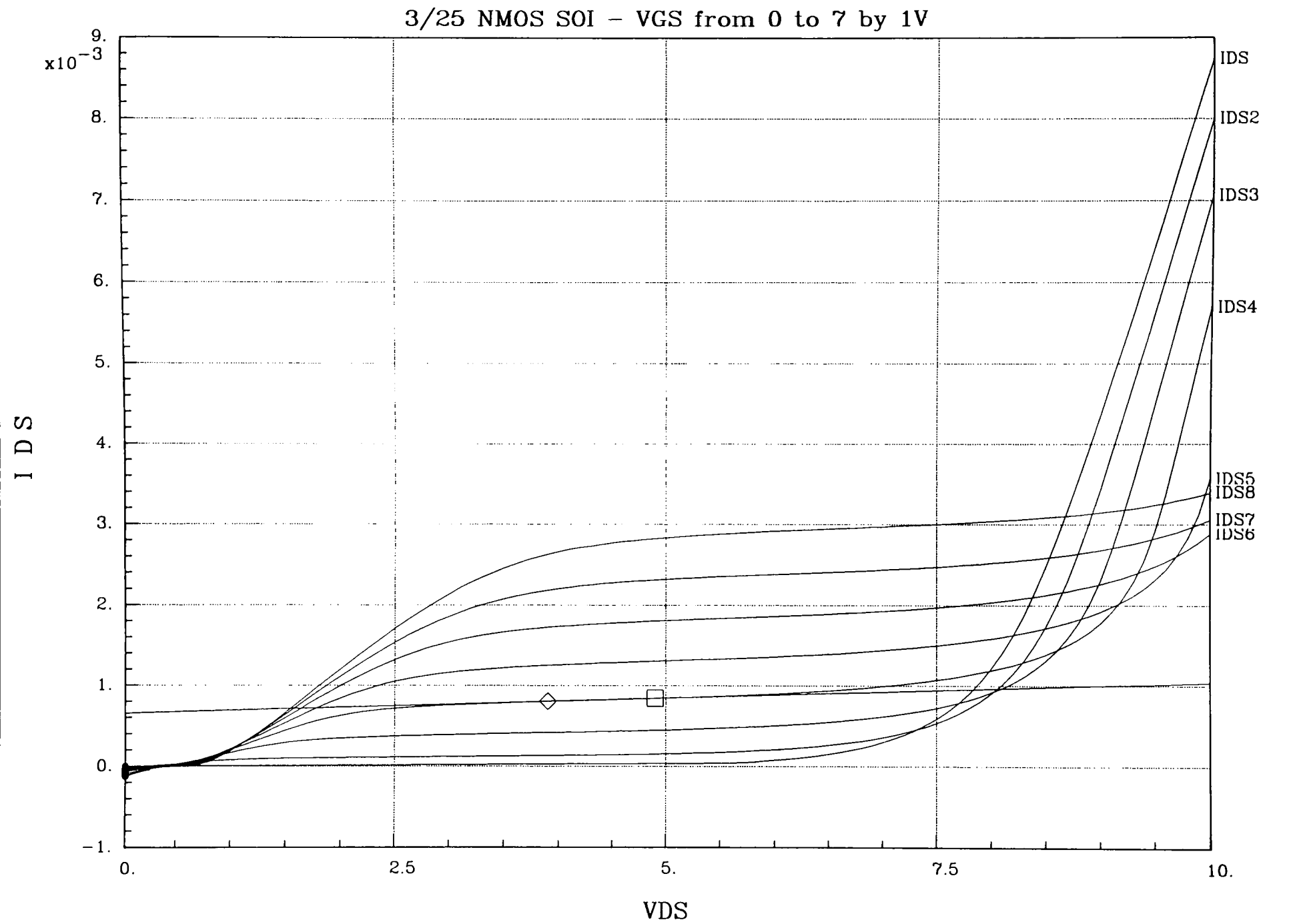
X1: -1.280 Y1: 2.9437m Slope: -4.4996m
X2: -1.6000 Y2: 4.3834m Y-int: -2.8158m
DX: 320.00m DY: -1.440m X-int: -625.8m

NMOS SOI

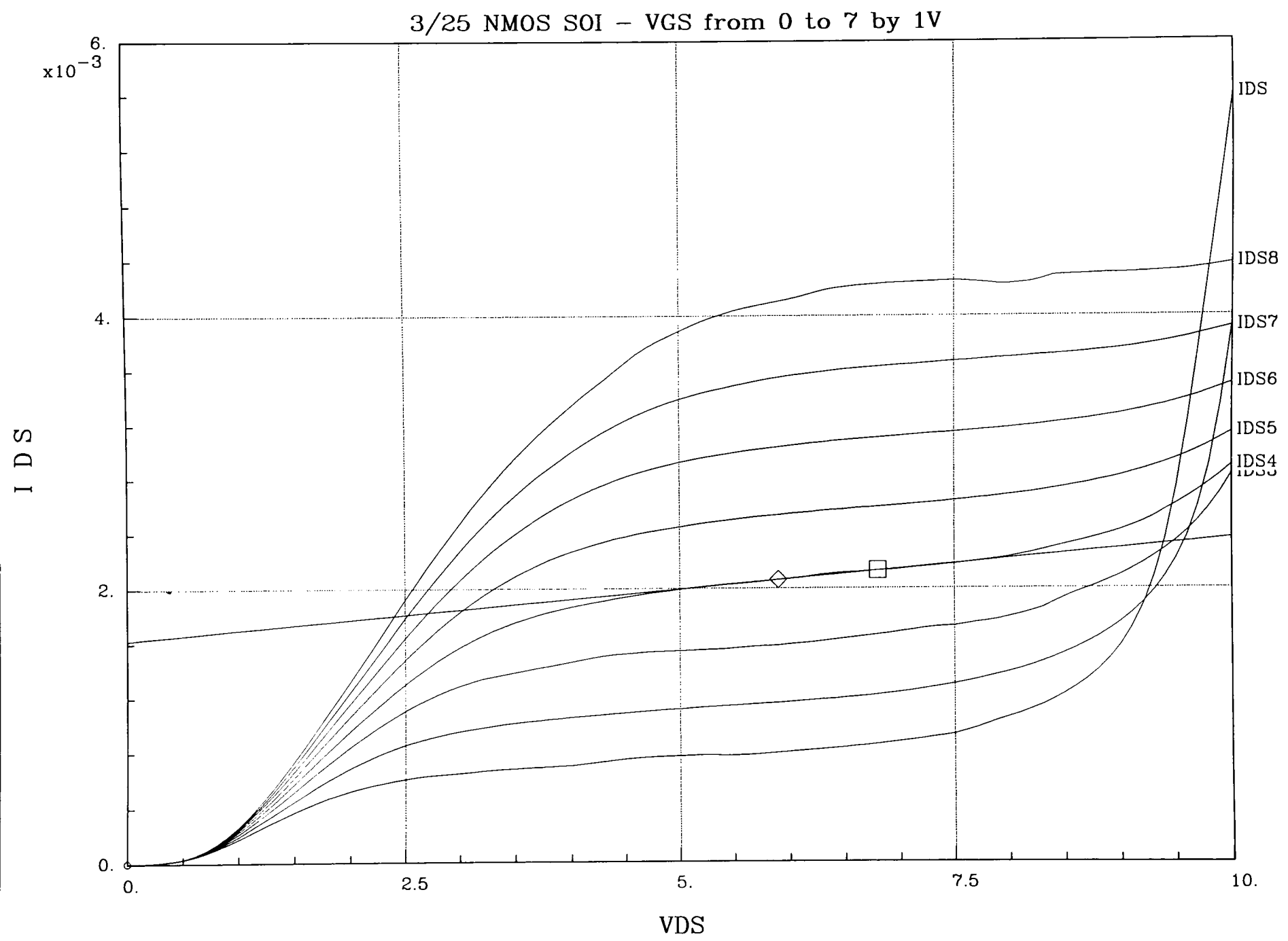
Device Parameter Extraction Curves



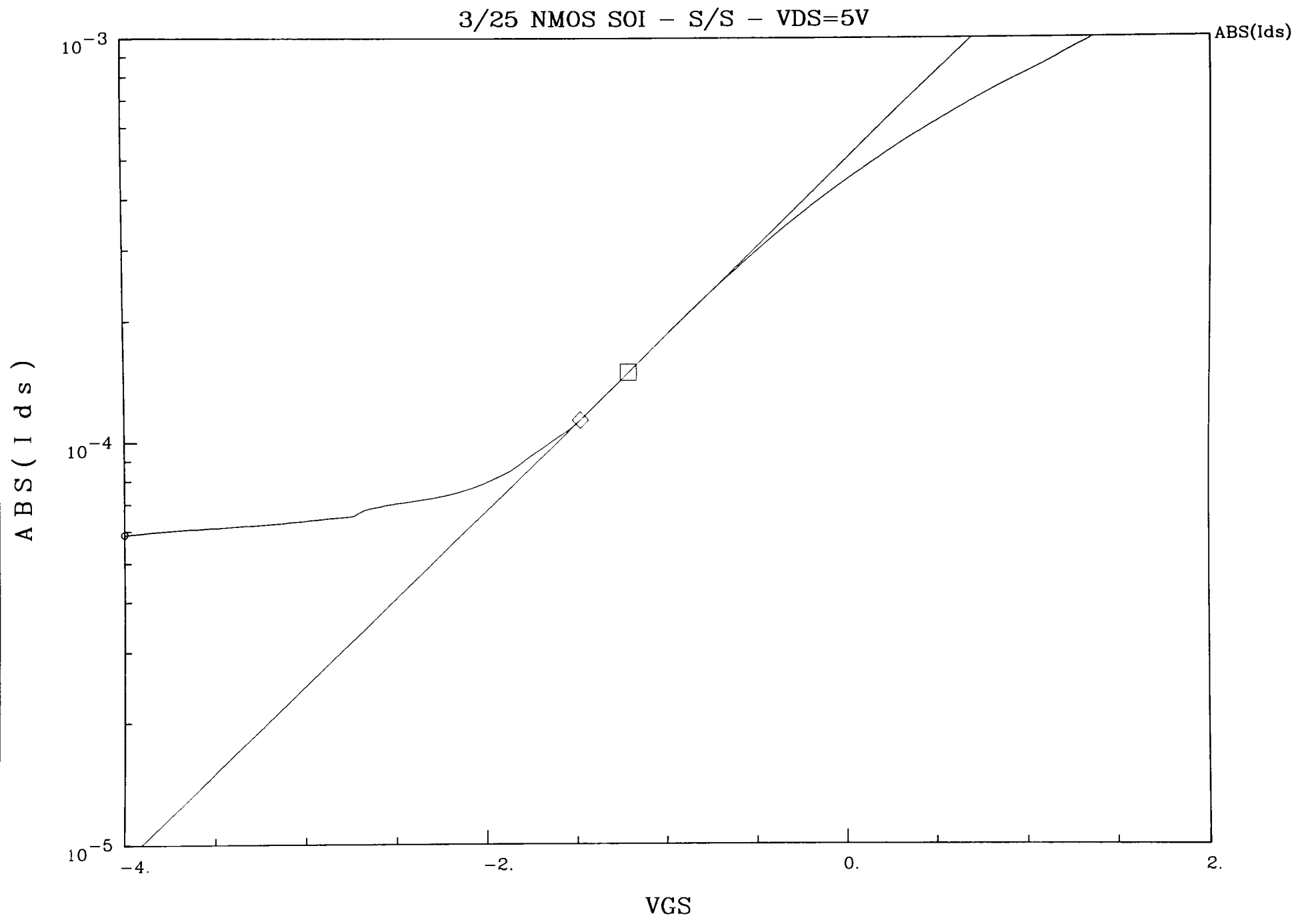
X1: 4.5000 Y1: 968.22u Slope: 44.061u
X2: 5.8000 Y2: 1.0256m Y-int: 769.94u
DX: -1.3000 DY: -57.280u X-int: -17.474



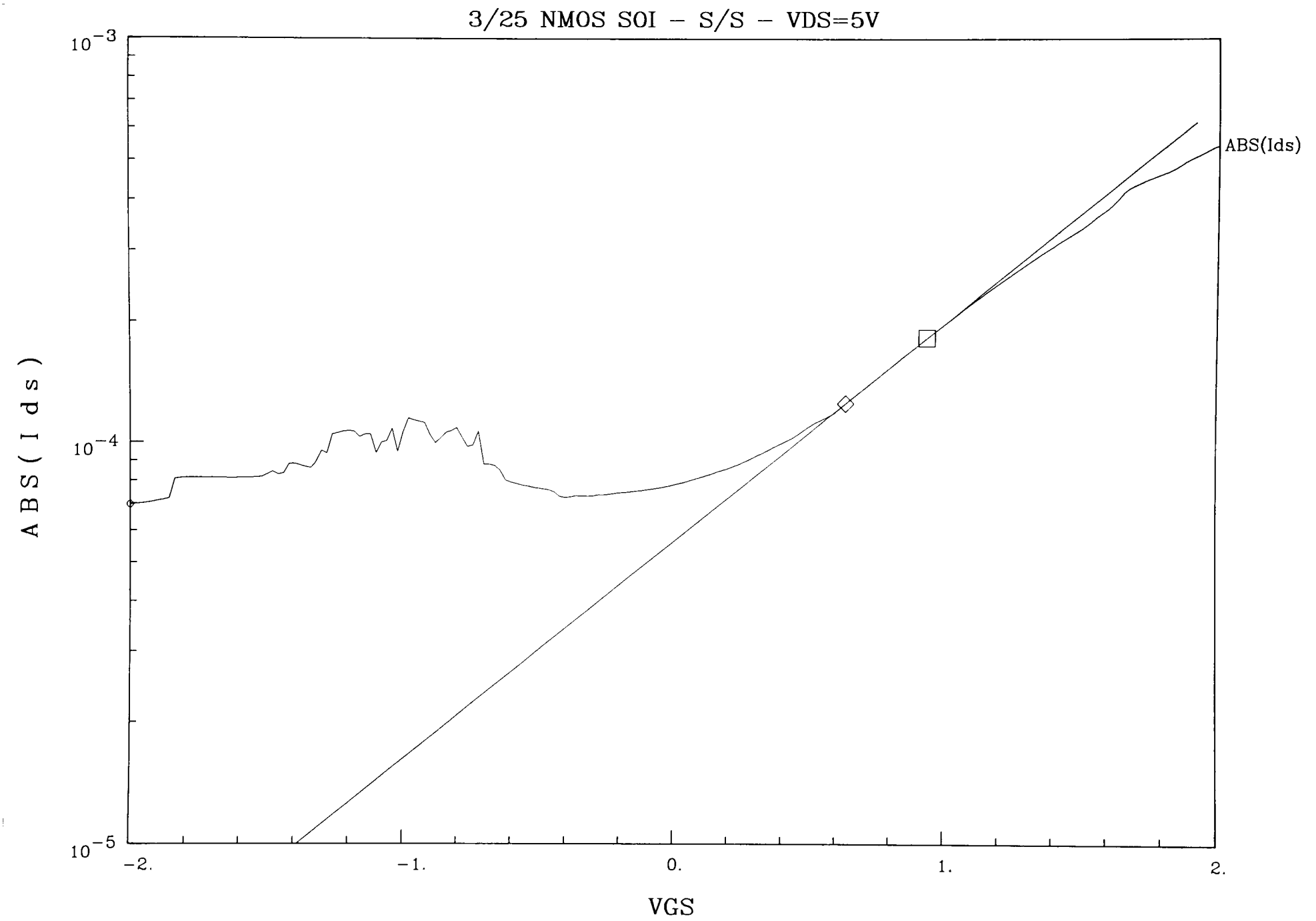
X1: 4.9000 Y1: 839.71u Slope: 38.420u
X2: 3.9000 Y2: 801.3u Y-int: 651.46u
DX: 1.0000 DY: 38.420u X-int: -16.957



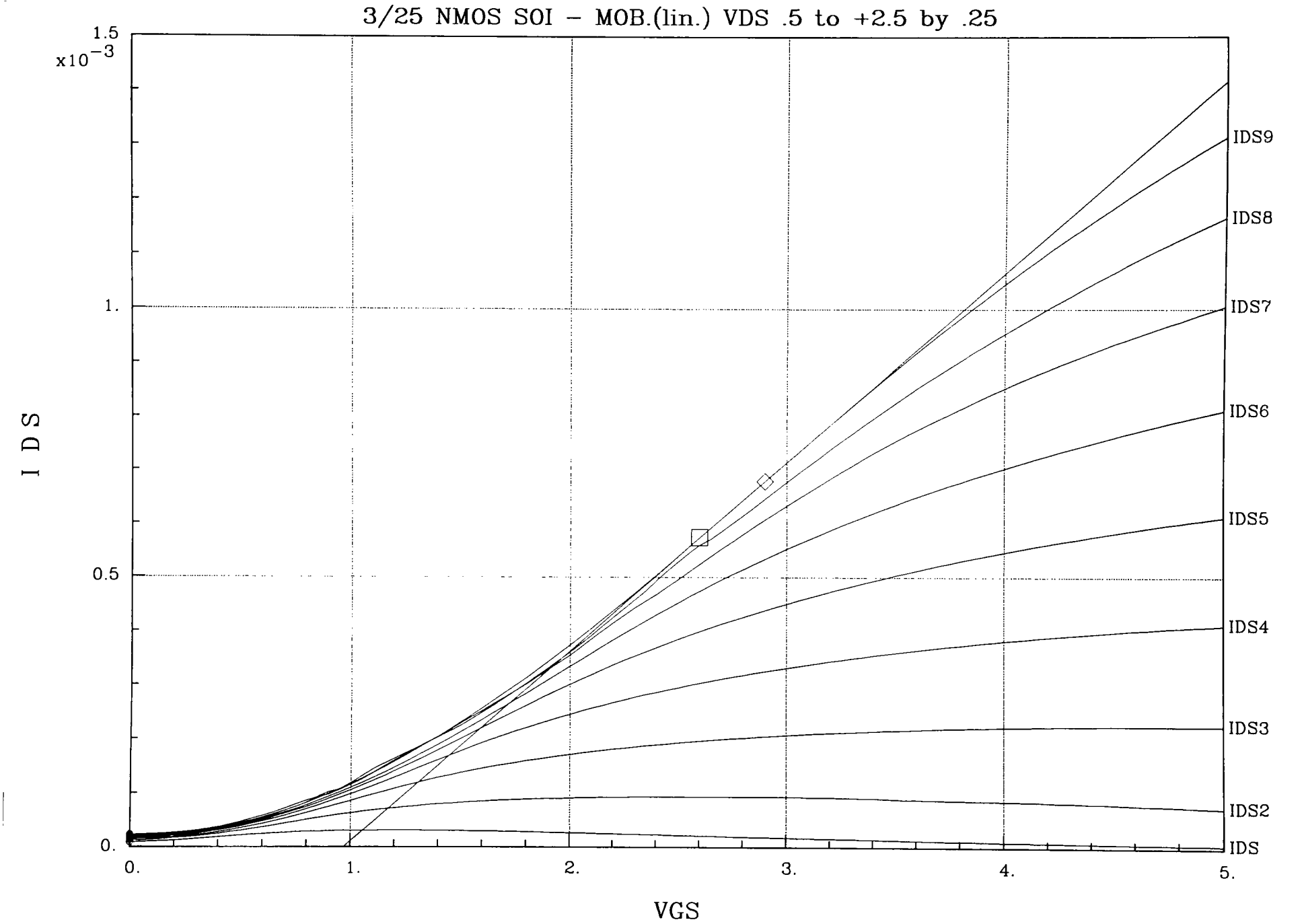
X1: 5.9000 Y1: 2.0604m Slope: 74.000u
X2: 6.8000 Y2: 2.1271m Y-int: 1.624m
DX: -900.00m DY: -66.600u X-int: -21.944



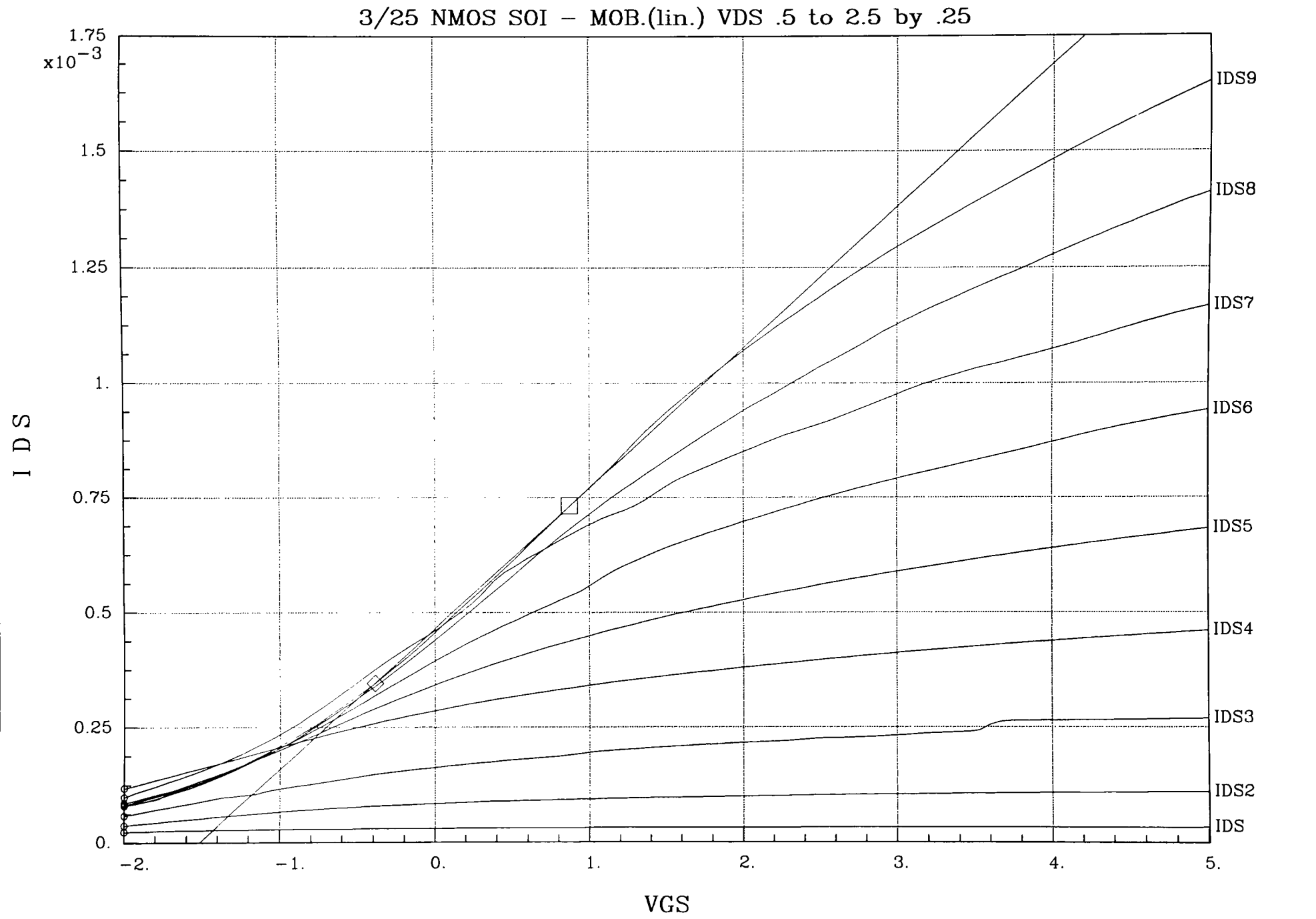
X1: −1.2100 Y1: 148.8u A: 499.80u
X2: −1.4800 Y2: 113.54u B: 1.0013
DX: 270.0m DY: 35.25u y = A*e~(B*x)



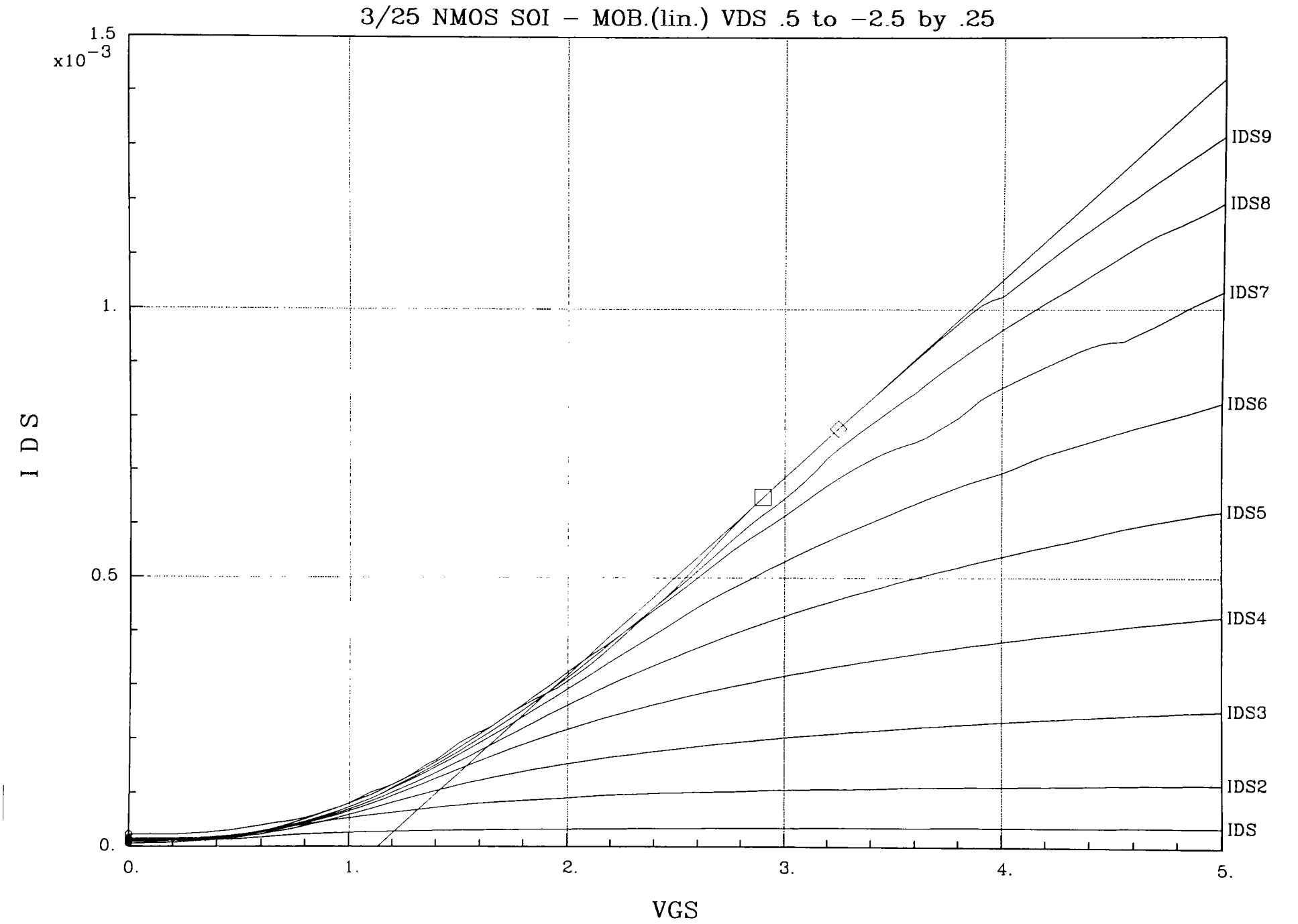
X1: 940.0m Y1: 182.41u A: 56.447u
X2: 640.0m Y2: 125.44u B: 1.248
DX: 300.00m DY: 56.960u y = A*e~(B*x)



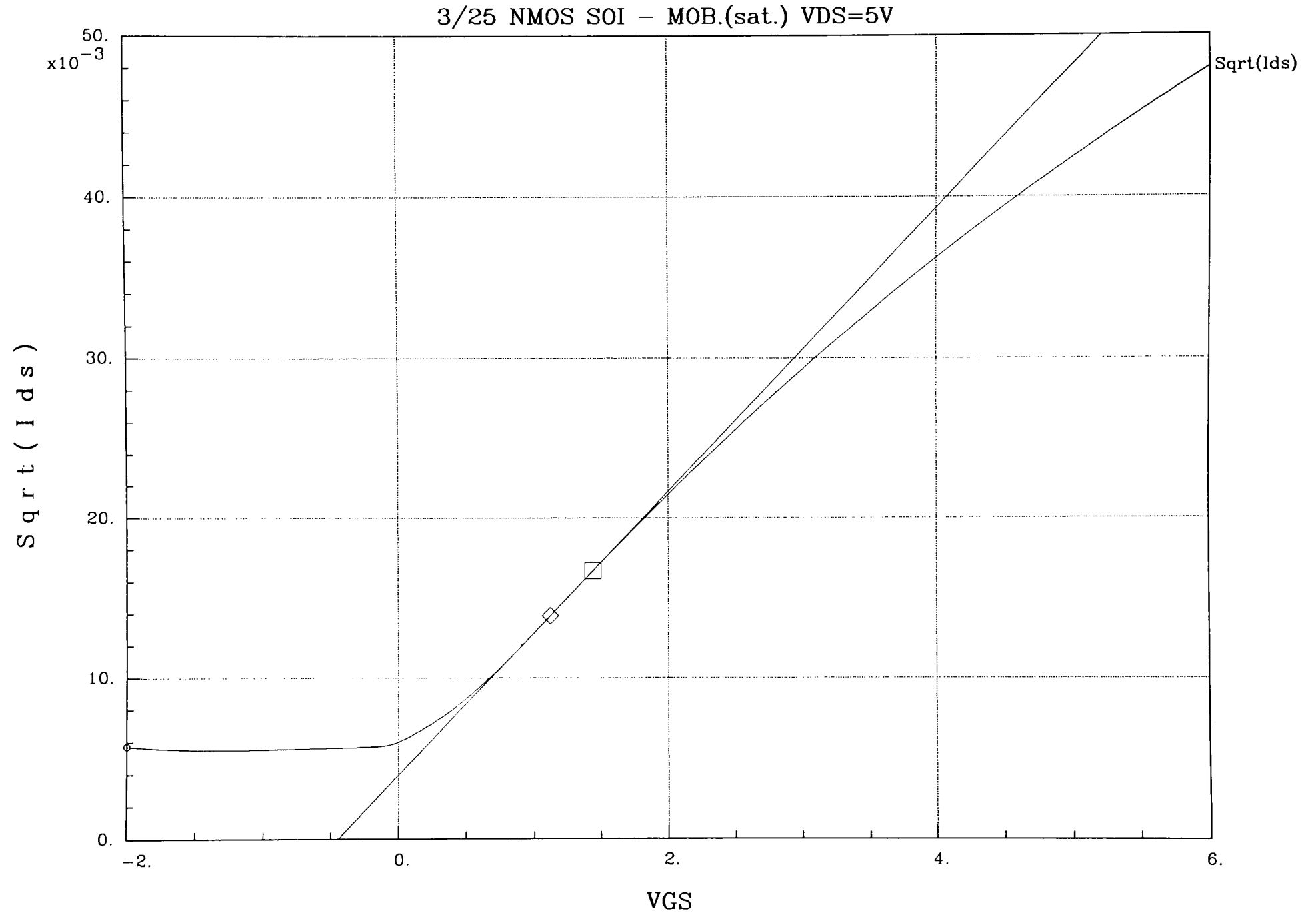
X1: 2.9000 Y1: 678.97u Slope: 351.67u
X2: 2.600 Y2: 573.47u Y–int: –340.88u
DX: 300.00m DY: 105.5u X–int: 969.30m



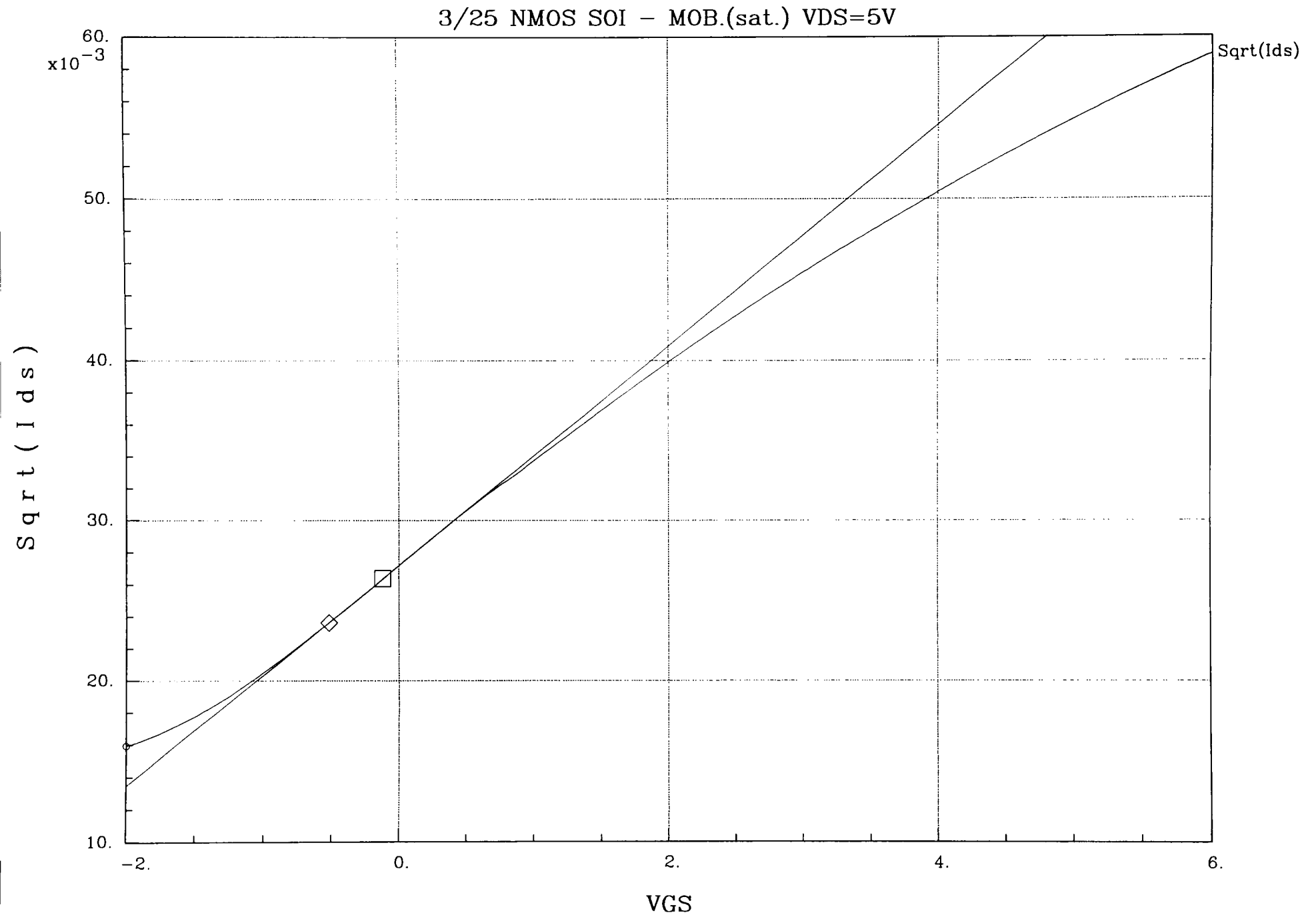
X1: 870.00m Y1: 730.84u Slope: 306.0u
X2: −390.0m Y2: 345.30u Y−int: 464.63u
DX: 1.260 DY: 385.54u X−int: −1.5184



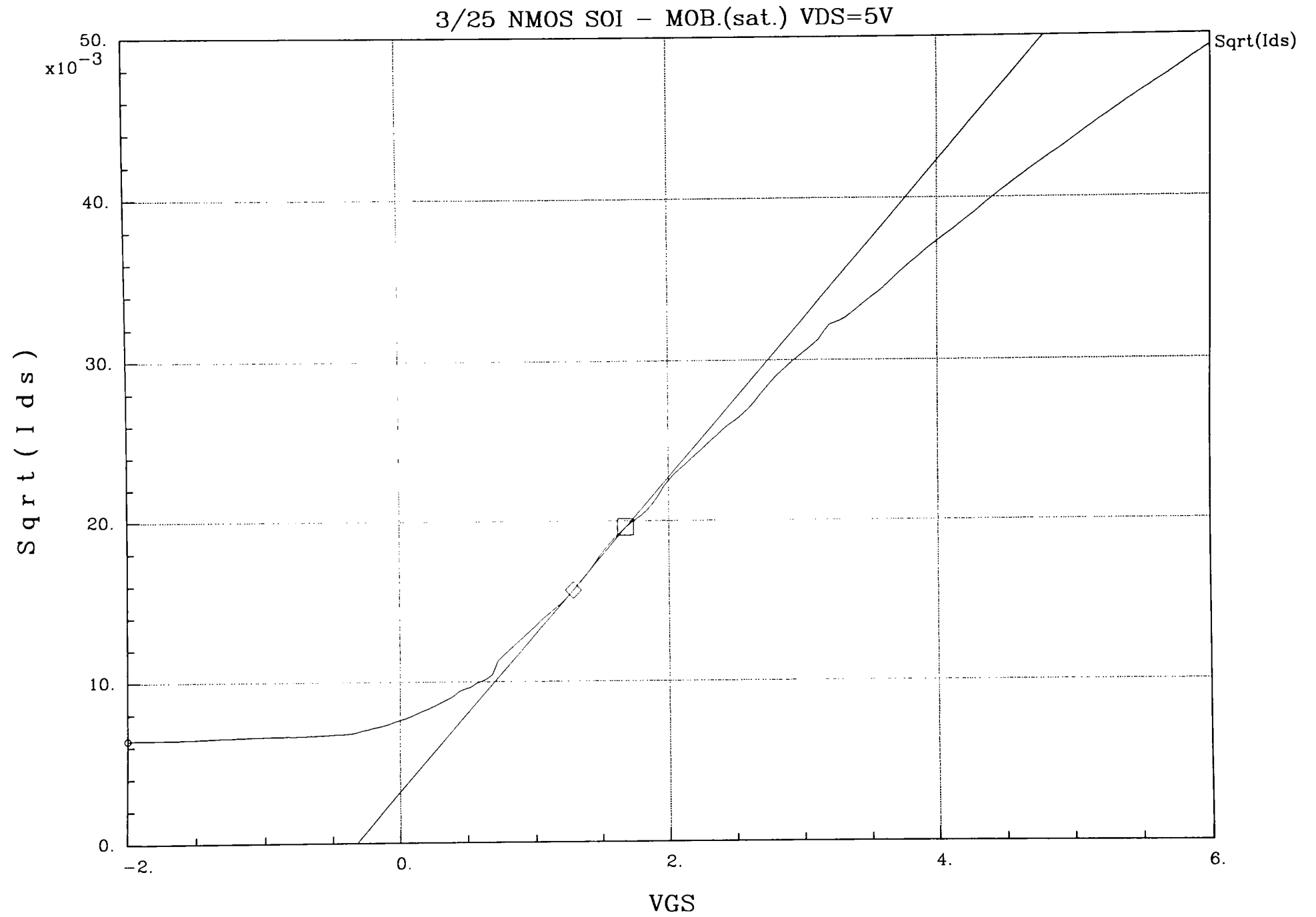
X1: 2.9000 Y1: 649.6u Slope: 367.60u
X2: 3.2500 Y2: 778.27u Y−int: −416.44u
DX: −350.0m DY: −128.67u X−int: 1.133



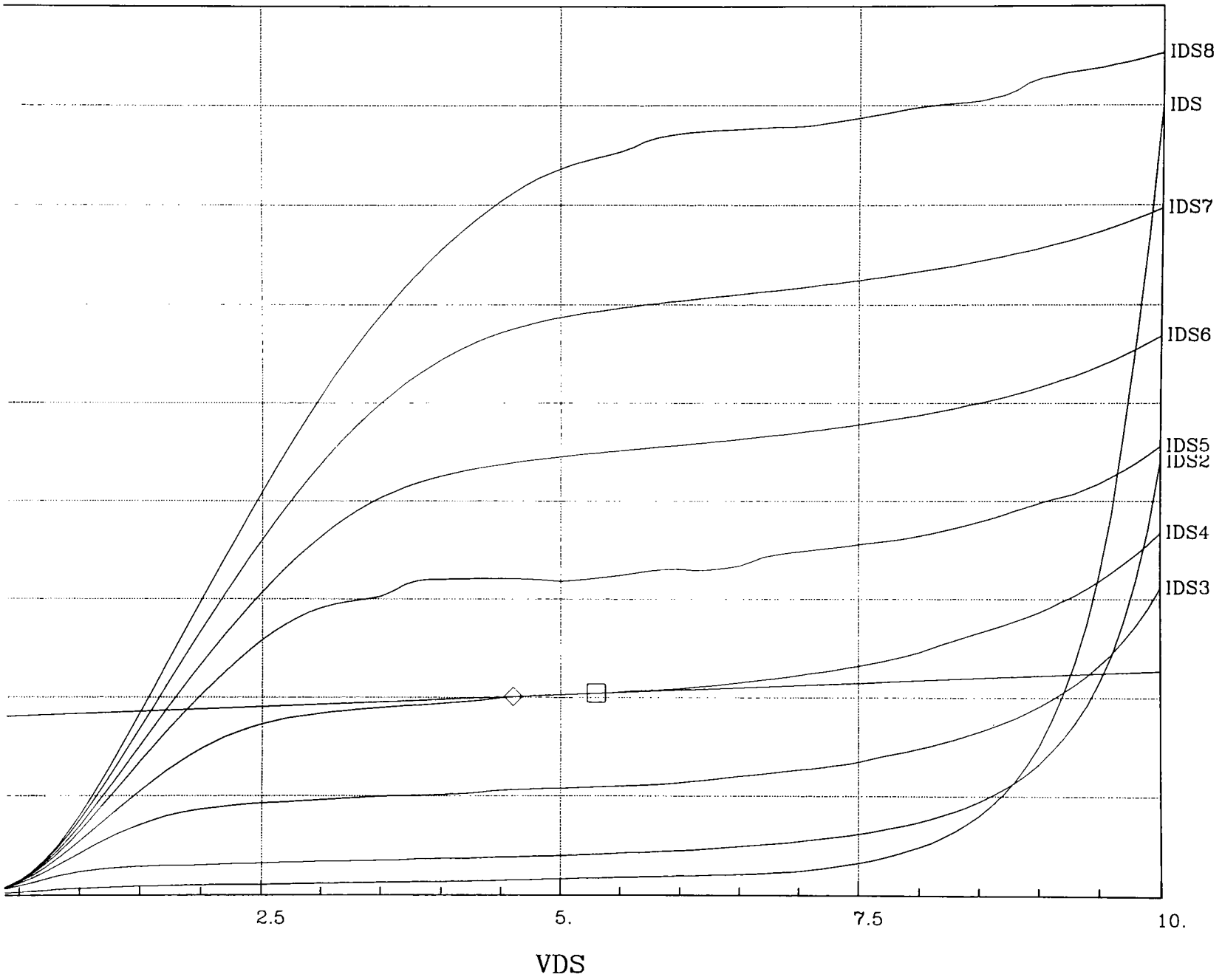
X1: 1.1200	Y1: 13.866m	Slope: 8.846m
X2: 1.4400	Y2: 16.697m	Y-int: 3.9580m
DX: -320.00m	DY: -2.8307m	X-int: -447.44m



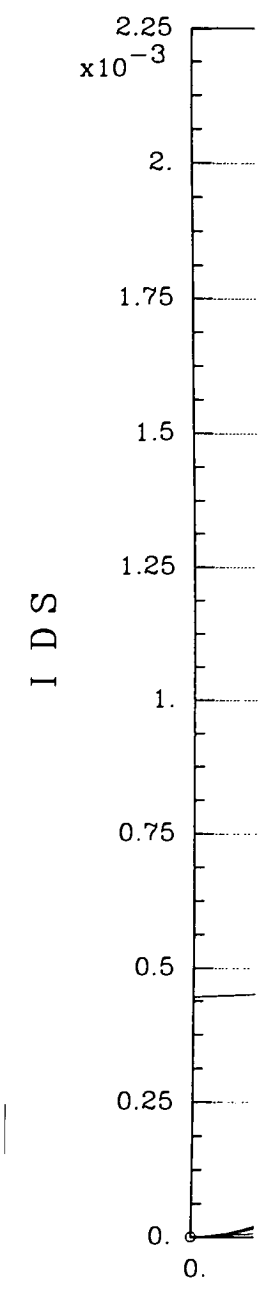
X1: −120.0m Y1: 26.36m Slope: 6.8487m
X2: −520.0m Y2: 23.62m Y−int: 27.18m
DX: 400.0m DY: 2.7394m X−int: −3.9687



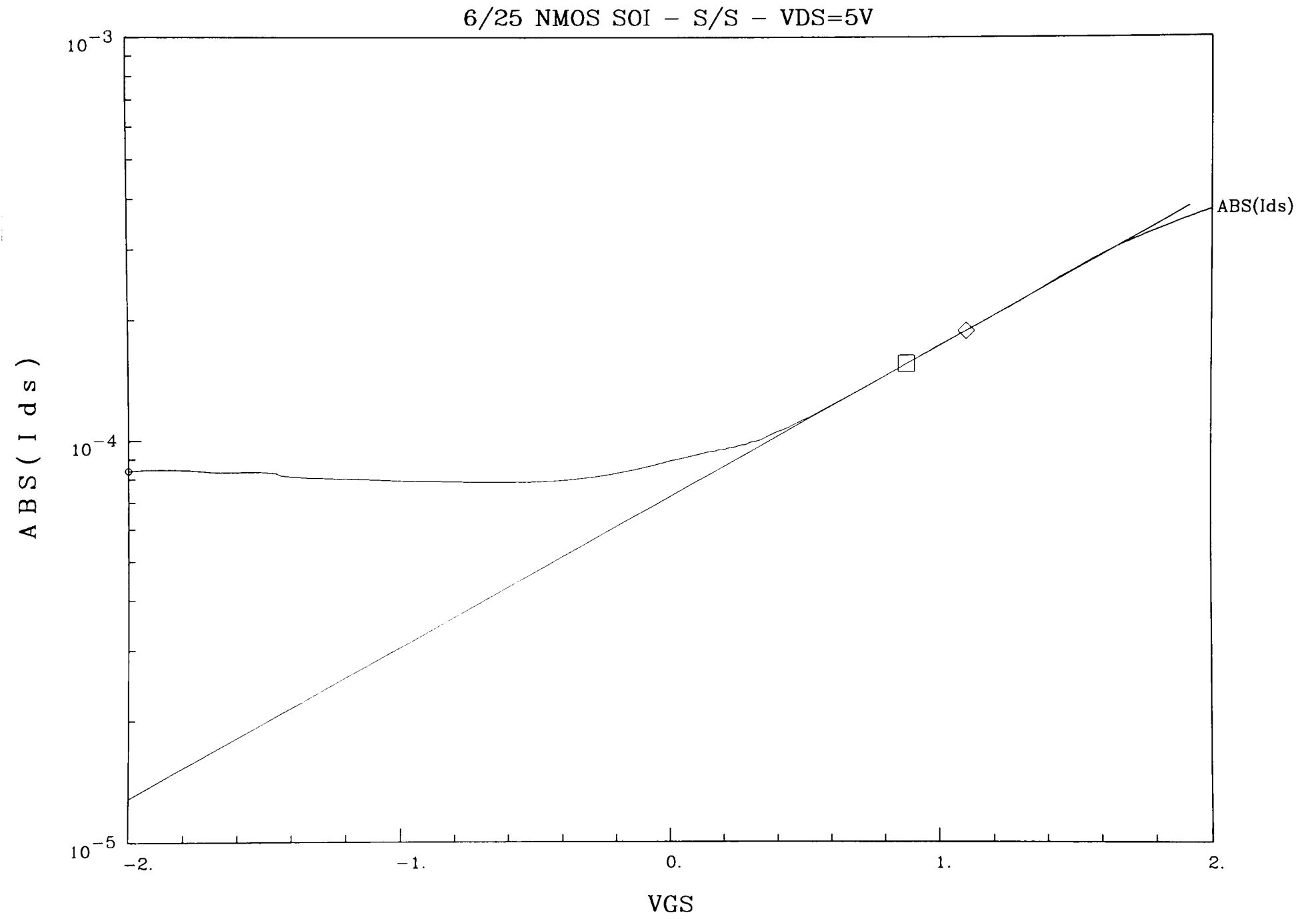
X1: 1.680 Y1: 19.60m Slope: 9.782m
X2: 1.280 Y2: 15.686m Y-int: 3.1652m
DX: 400.0m DY: 3.9128m X-int: -323.58m



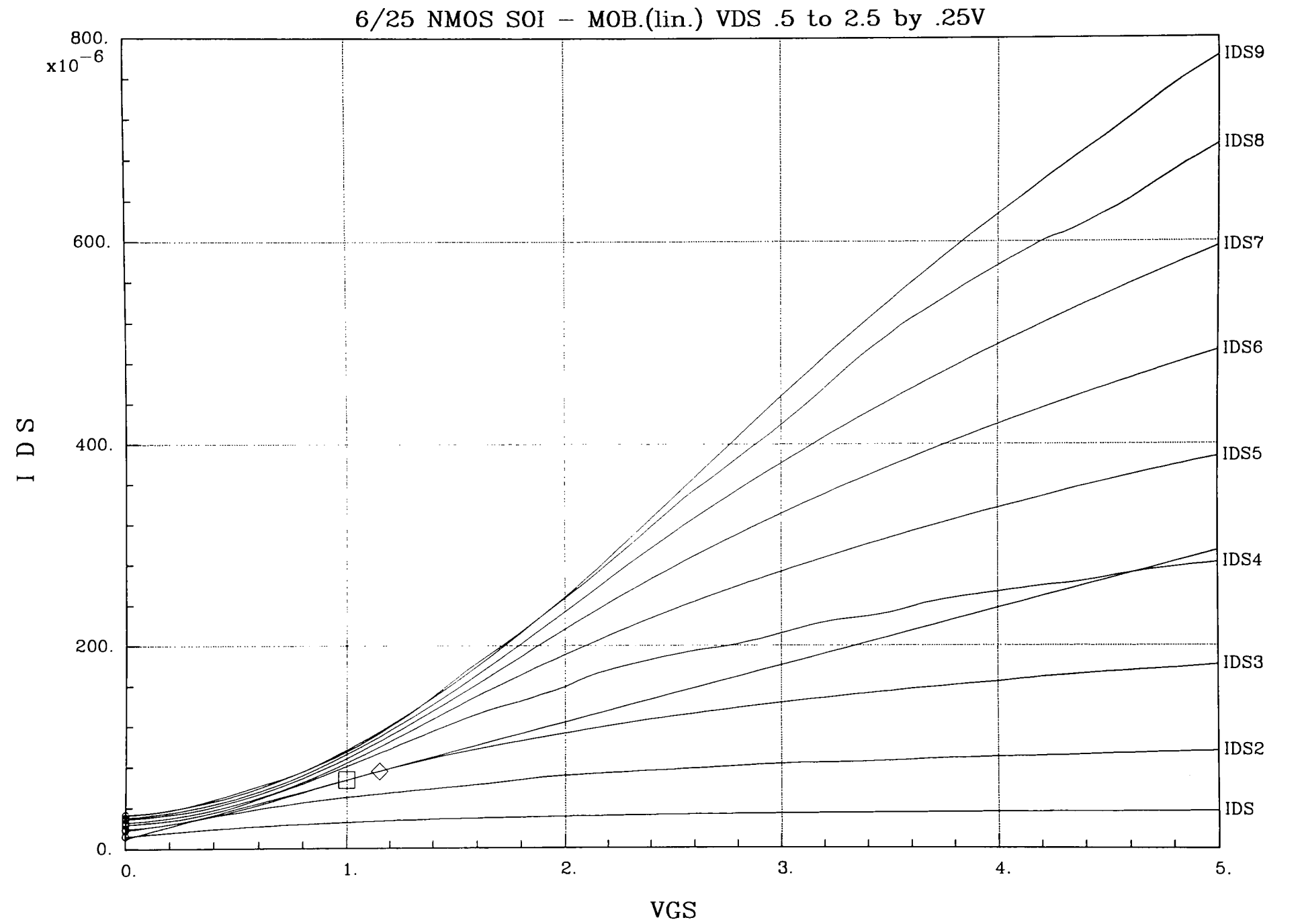
Y1: 500.94u Slope: 12.13u
Y2: 509.44u Y-int: 445.16u
DY: -8.4900u X-int: -36.703



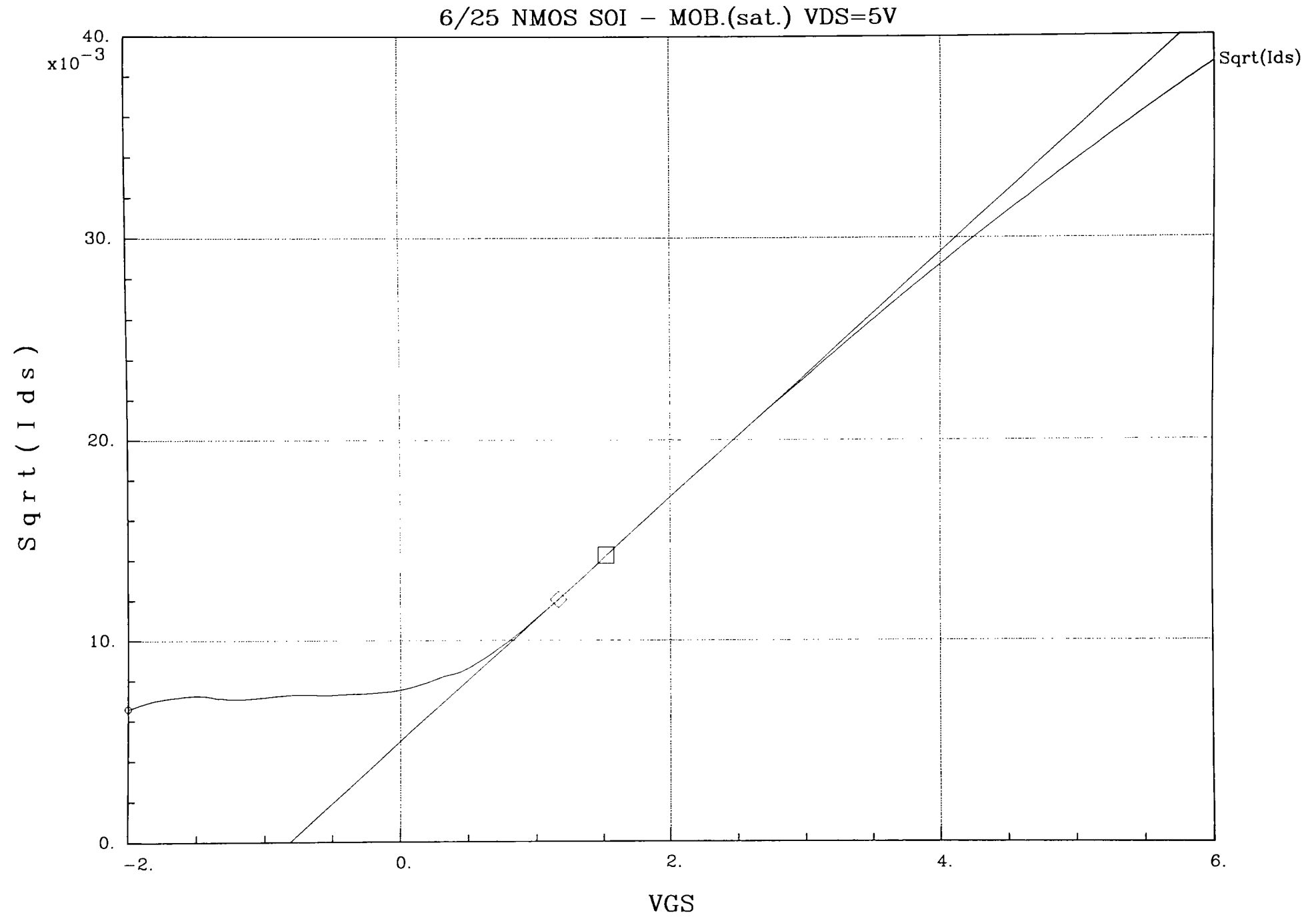
X1: 4.600
X2: 5.3000
DX: −700.00m



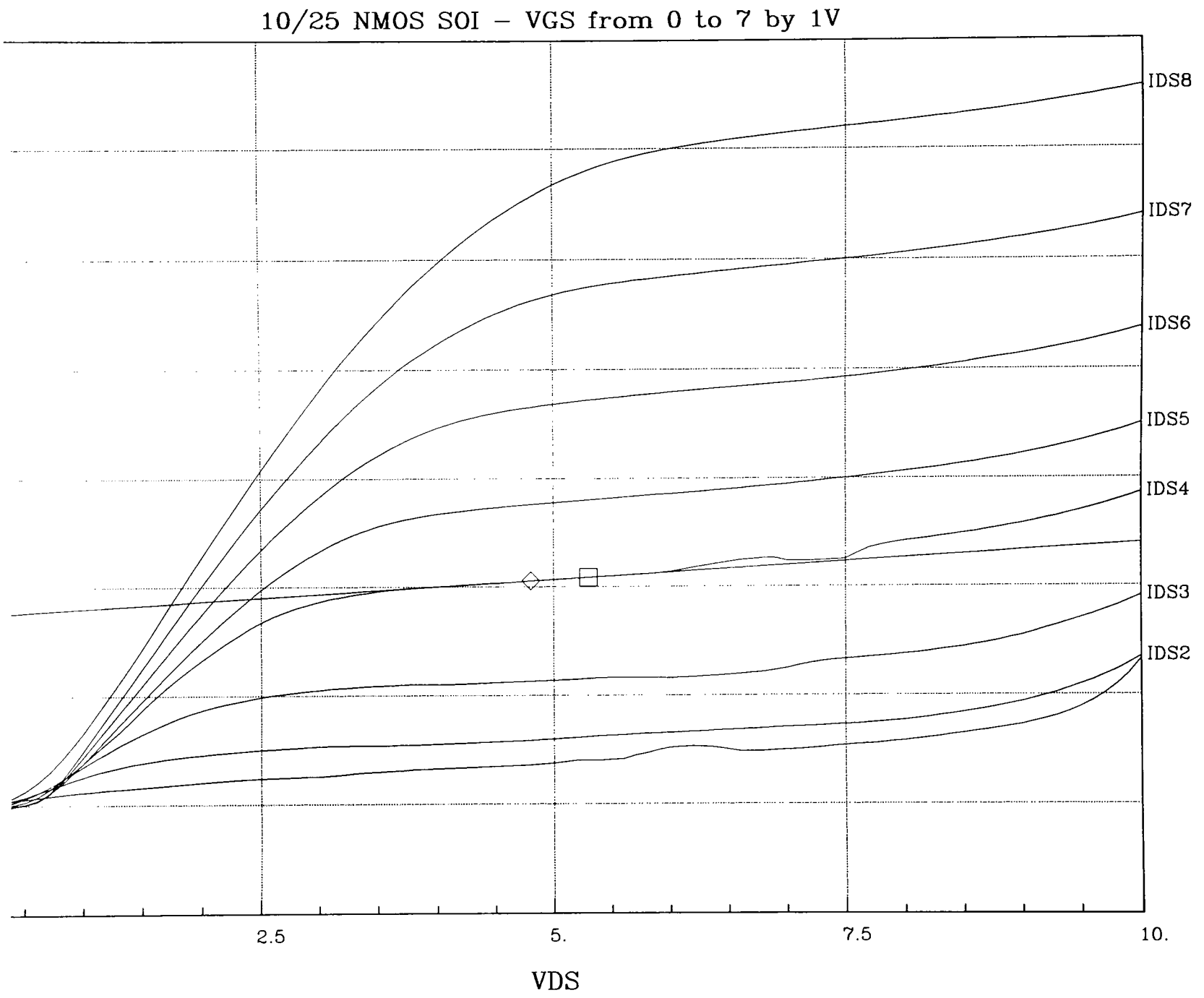
X1: 880.0m Y1: 155.40u A: 72.548u
X2: 1.1000 Y2: 188.00u B: 865.63m
DX: −220.00m DY: −32.600u y = A*e~(B*x)



X1: 1.150 Y1: 75.46u Slope: 56.693u
X2: 1.0000 Y2: 66.954u Y-int: 10.261u
DX: 150.0m DY: 8.5040u X-int: -181.00m

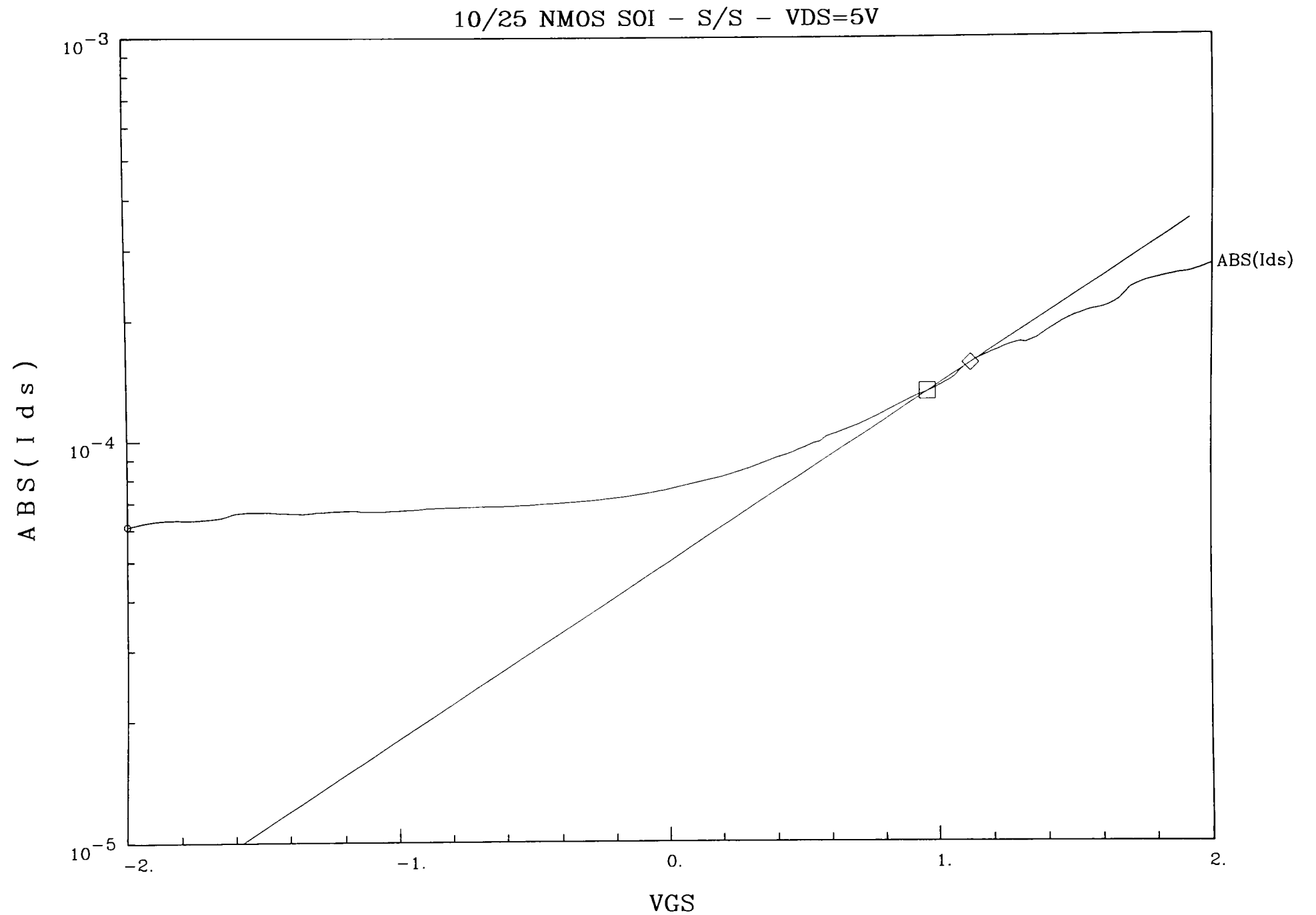


X1: 1.520 Y1: 14.223m Slope: 6.089m
X2: 1.160 Y2: 12.031m Y-int: 4.9680m
DX: 360.00m DY: 2.1920m X-int: −815.91m

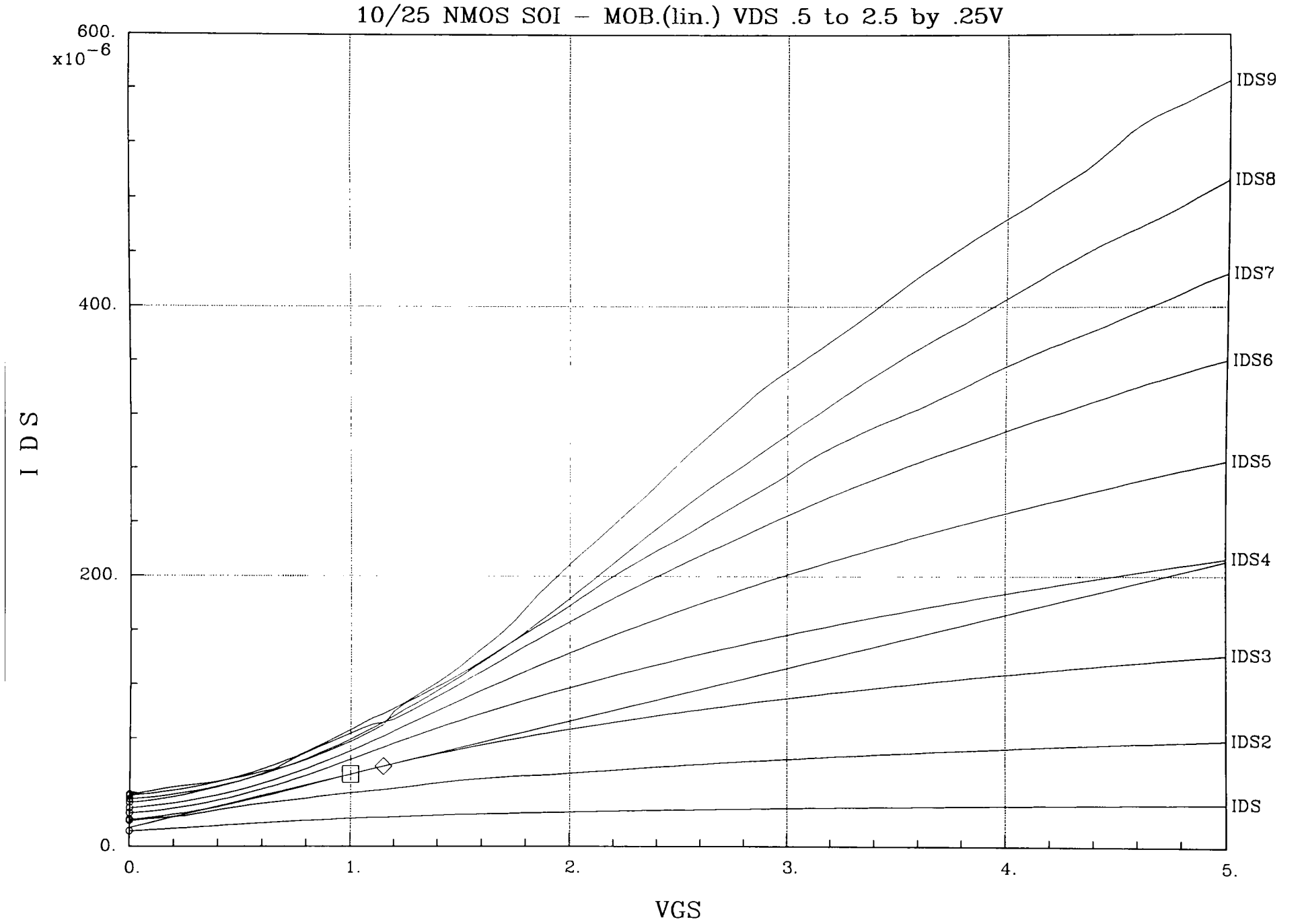


Y1: 520.77u
Y2: 512.51u
DY: 8.260u

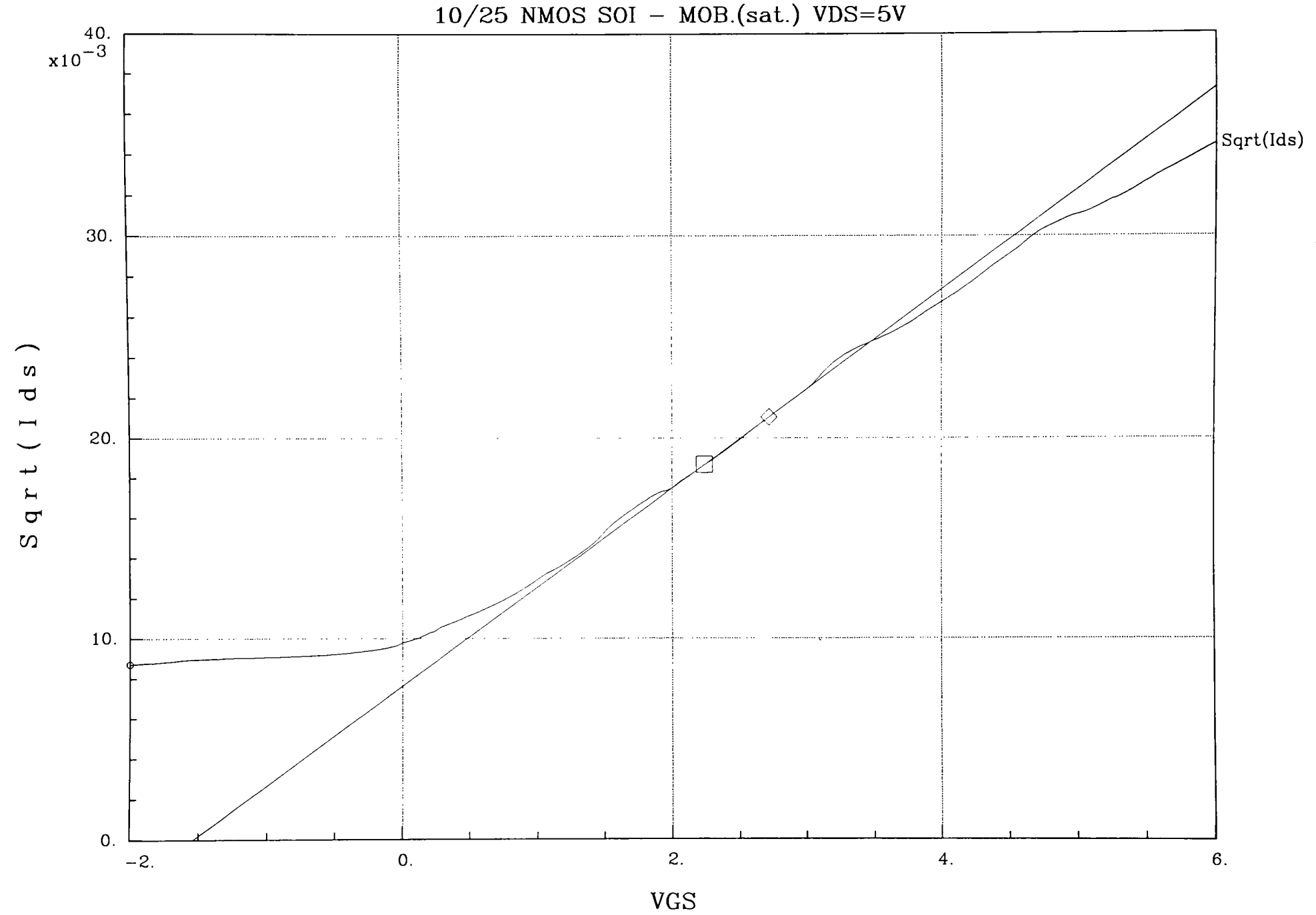
Slope: 16.52u
Y-int: 433.21u
X-int: -26.223



X1: 960.0m Y1: 132.30u A: 49.796u
X2: 1.1200 Y2: 155.70u B: 1.018
DX: −160.00m DY: −23.400u y = A*e~(B*x)



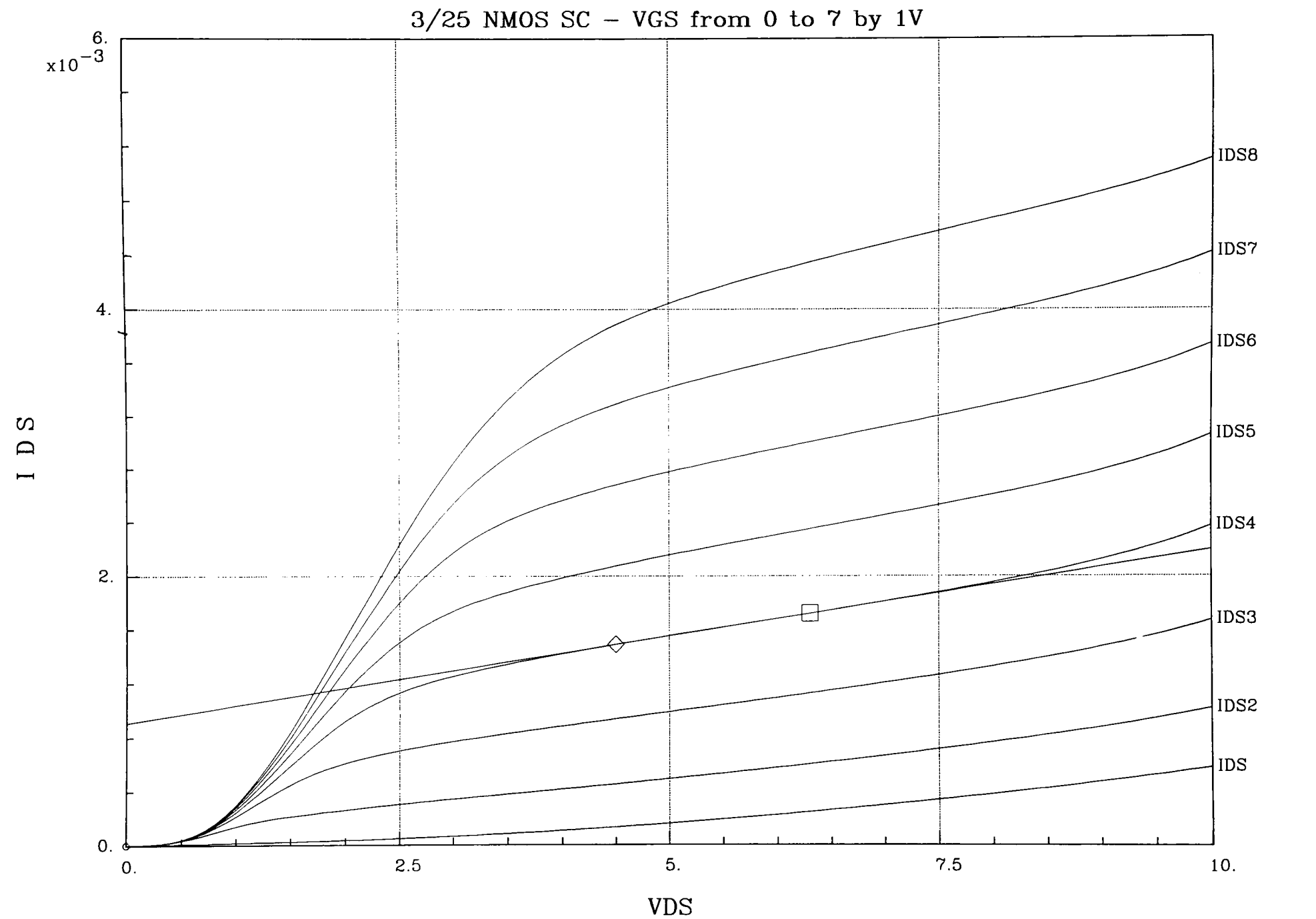
X1: 1.150 Y1: 59.03u Slope: 39.367u
X2: 1.0000 Y2: 53.124u Y-int: 13.758u
DX: 150.0m DY: 5.905u X-int: -349.47m



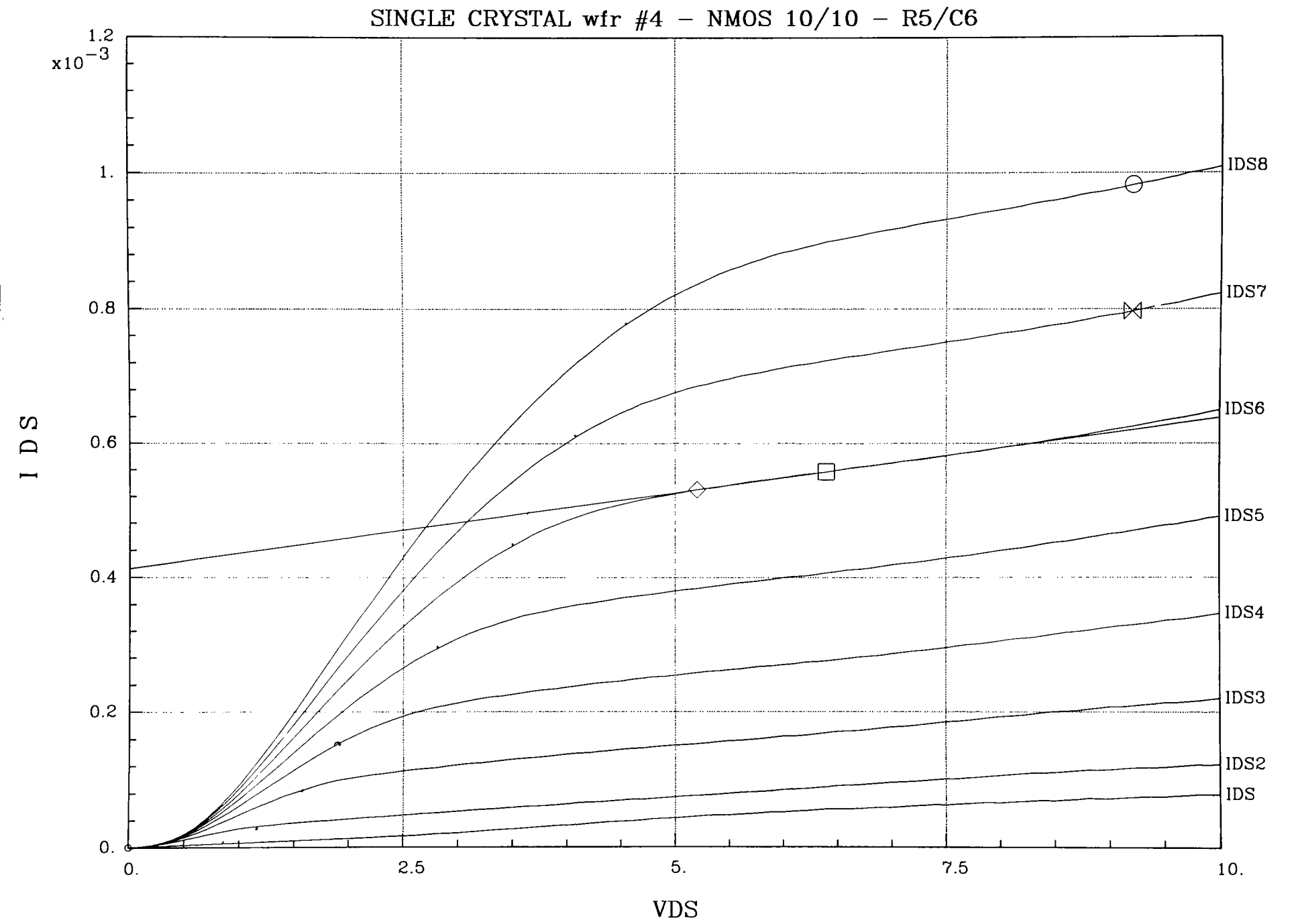
X1: 2.7200 Y1: 21.04m Slope: 4.9392m
X2: 2.2400 Y2: 18.67m Y-int: 7.6046m
DX: 480.00m DY: 2.371m X-int: -1.5397

NMOS SINGLE CRYSTAL

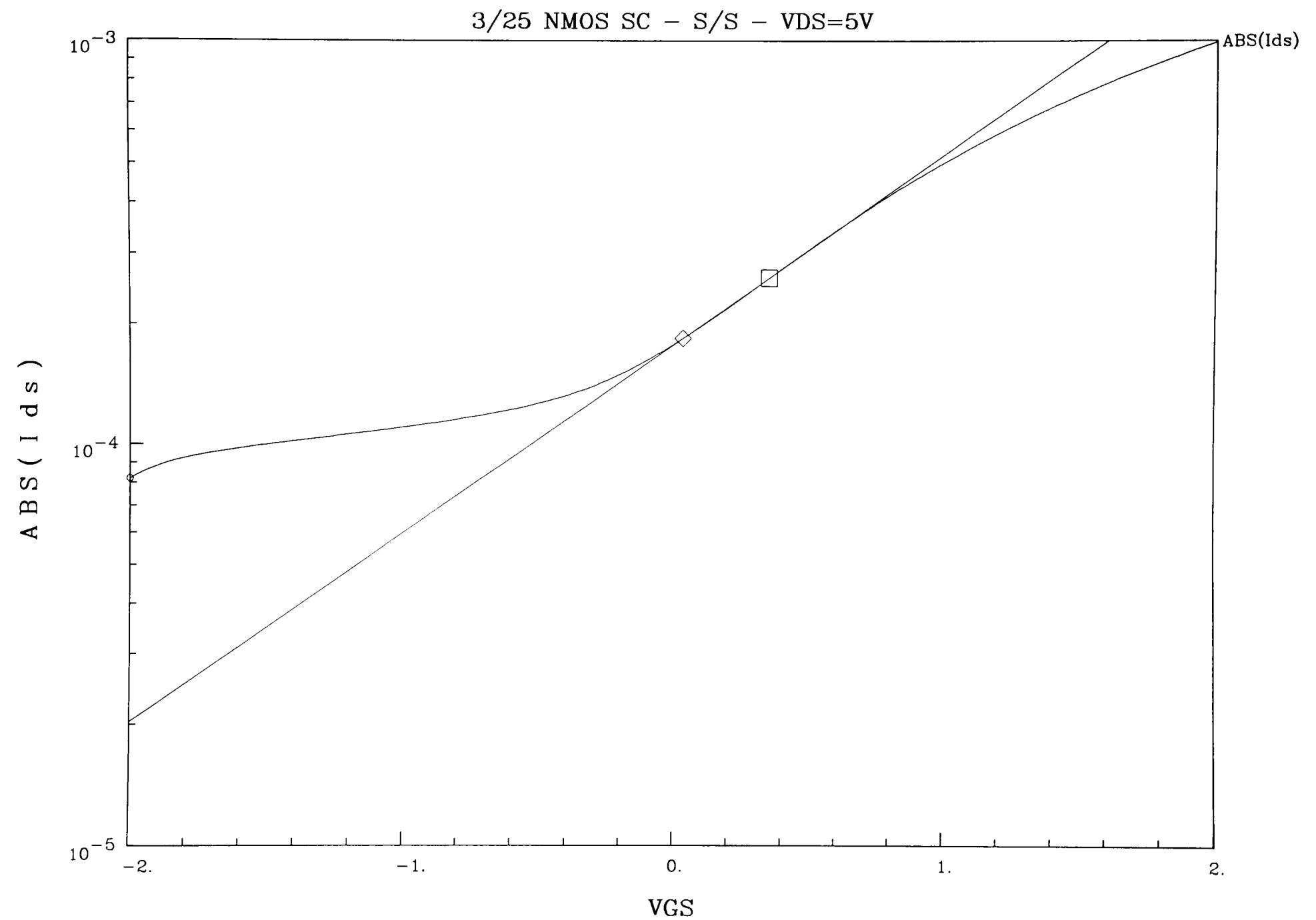
Device Parameter Extraction Curves



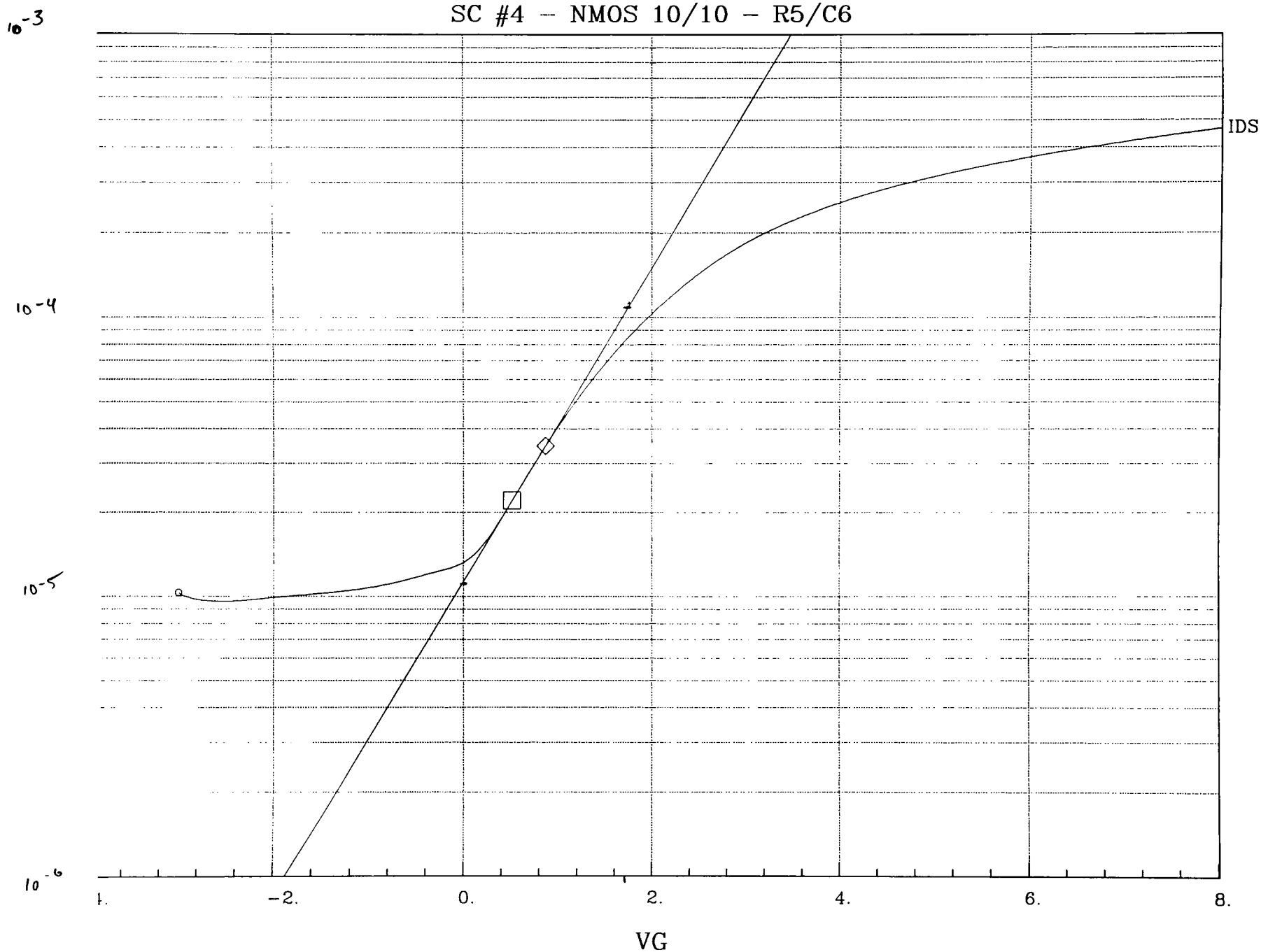
X1: 4.5000 Y1: 1.4870m Slope: 128.9u
X2: 6.3000 Y2: 1.7190m Y-int: 907.00u
DX: -1.8000 DY: -232.00u X-int: -7.0370



X1: 5.200 Y1: 530.1u Slope: 22.50u
X2: 6.4000 Y2: 557.1u Y-int: 413.1u
DX: -1.2000 DY: -27.00u X-int: -18.36



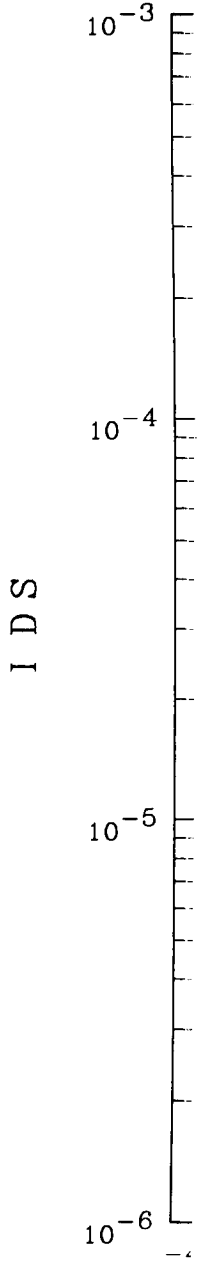
X1: 360.00m Y1: 260.50u A: 176.50u
X2: 40.00m Y2: 184.31u B: 1.0811
DX: 320.00m DY: 76.190u y = A*e~(B*x)



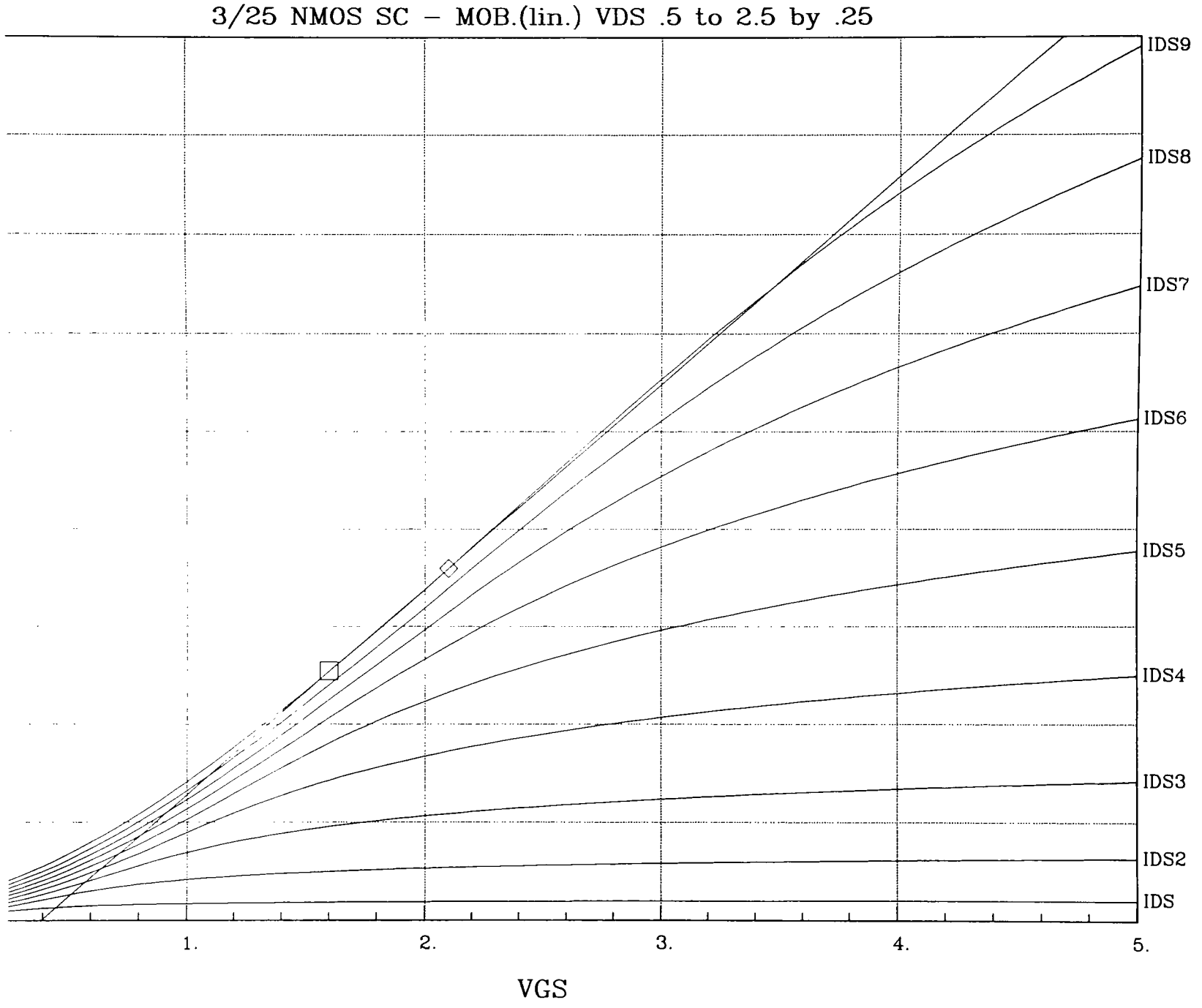
Y1: 34.574u
Y2: 21.964u
DY: 12.610u

A: 11.318u
B: 1.2912
y = A*e~(B*x)

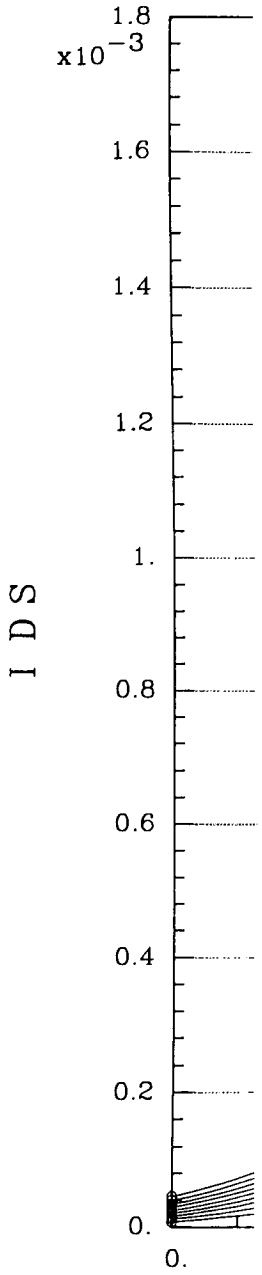
1.9V/decade



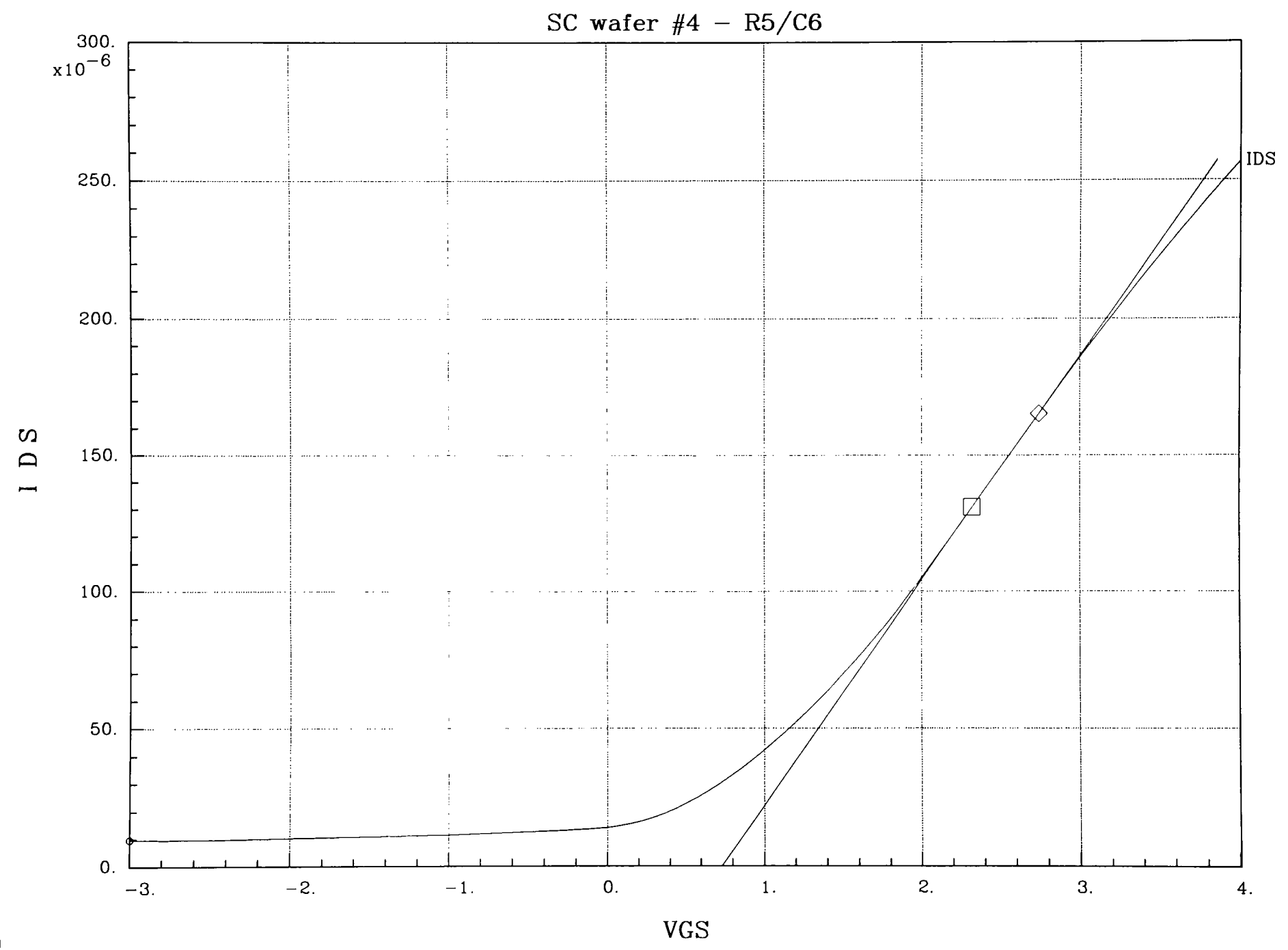
X1: 864.87m
X2: 513.51m
DX: 351.36m



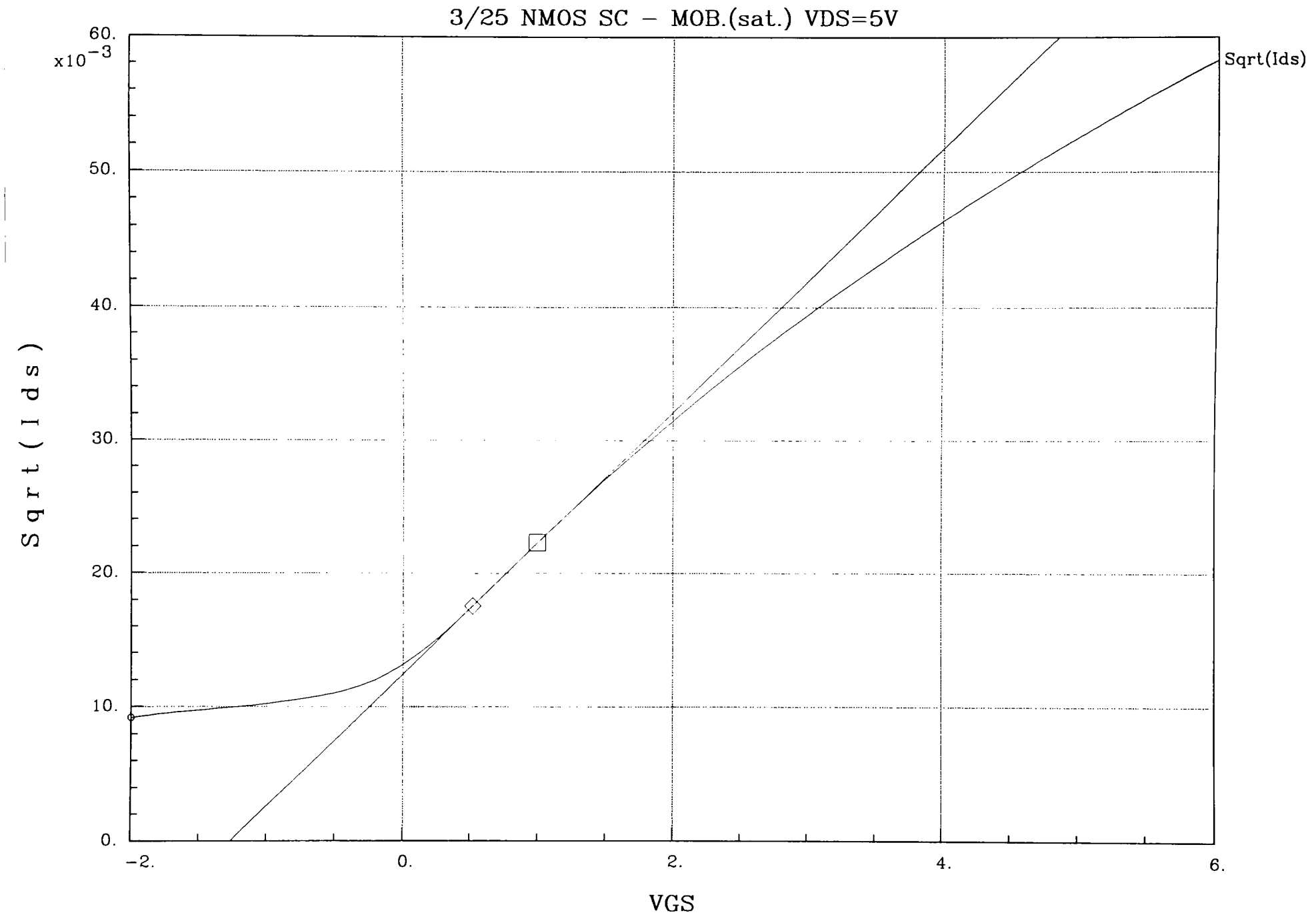
1: 507.66u Slope: 420.10u
2: 717.7u Y-int: −164.51u
Y: −210.04u X-int: 391.6m



X1: 1.6000 Y
X2: 2.100 Y
DX: −500.0m D



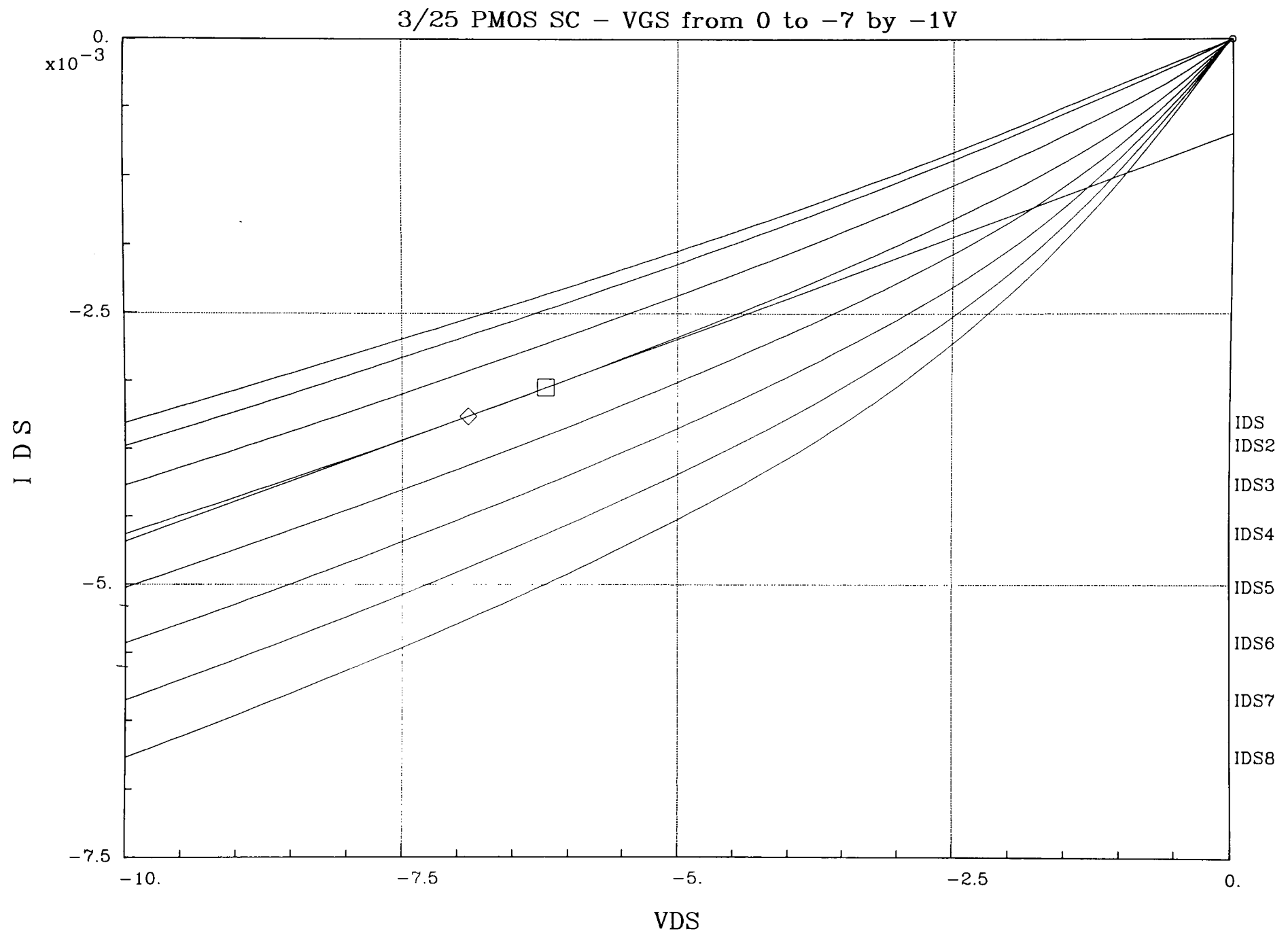
X1: 2.320 Y1: 130.66u Slope: 82.261u
X2: 2.7400 Y2: 165.20u Y-int: −60.198u
DX: −420.00m DY: −34.550u X-int: 731.78m



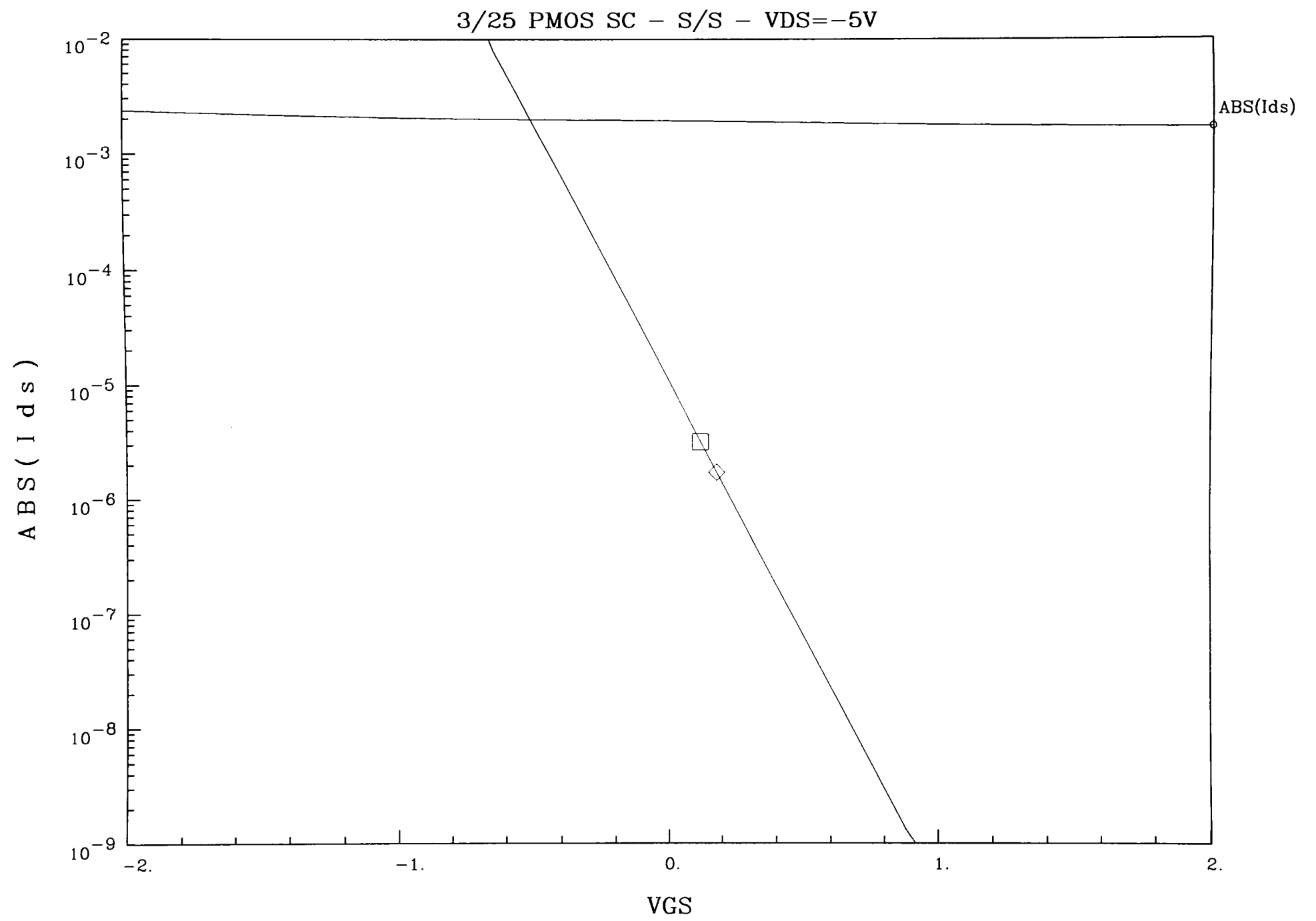
X1: 1.0000 Y1: 22.260m Slope: 9.832m
X2: 520.0m Y2: 17.541m Y-int: 12.43m
DX: 480.00m DY: 4.7192m X-int: -1.2641

PMOS SINGLE CRYSTAL

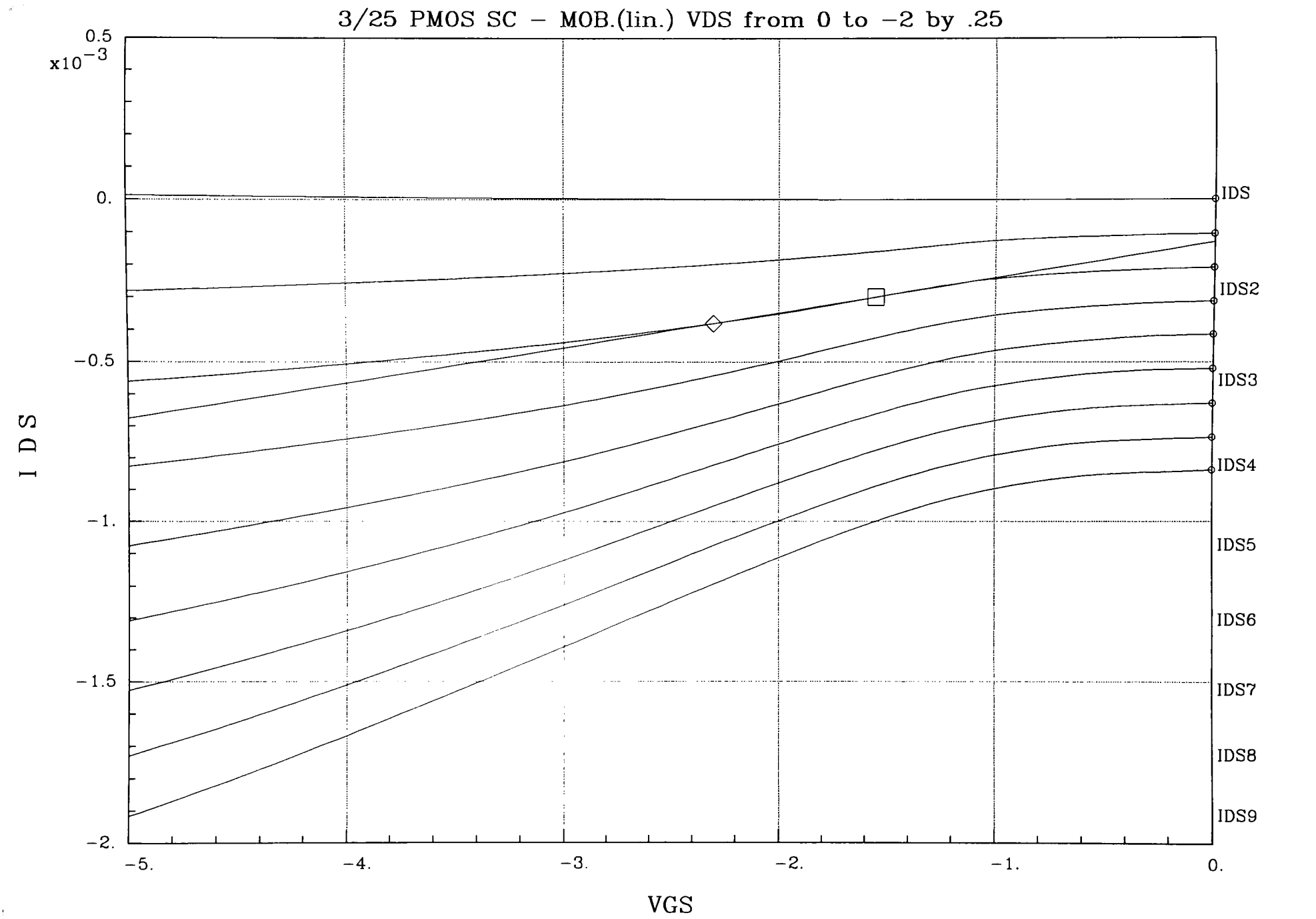
Device Parameter Extraction Curves



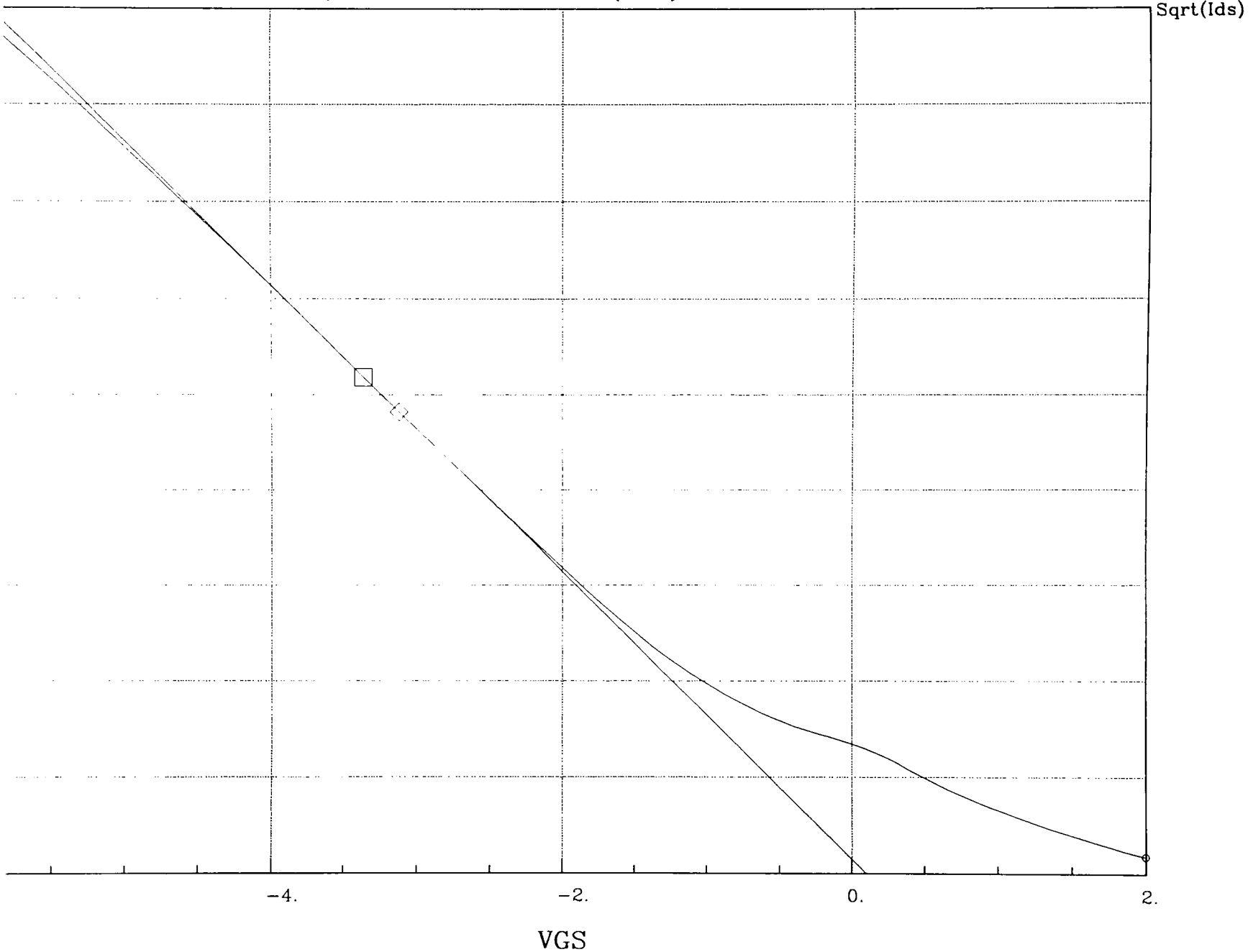
X1: −6.200 Y1: −3.1860m Slope: 373.58u
X2: −6.9000 Y2: −3.4476m Y−int: −869.86u
DX: 700.00m DY: 261.50u X−int: 2.3284



X1: 180.00m Y1: 1.722u A: 10.926u
X2: 120.0m Y2: 3.188u B: −10.264
DX: 60.000m DY: −1.466u y = A*e~(B*x)

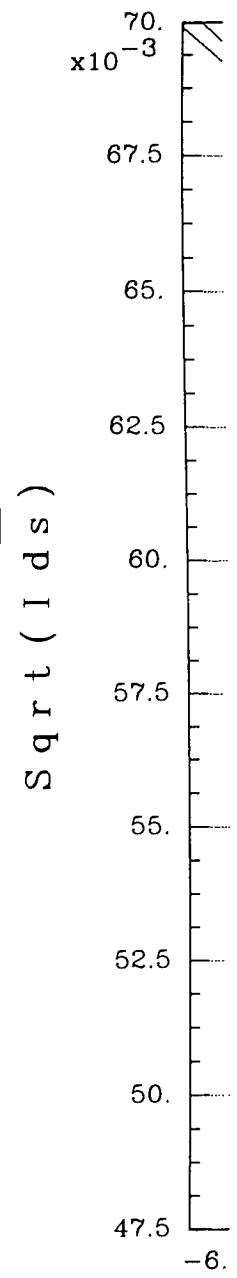


X1: −2.300 Y1: −381.31u Slope: 109.00u
X2: −1.550 Y2: −299.56u Y−int: −130.60u
DX: −750.00m DY: −81.750u X−int: 1.1982



Y1: 59.552m
Y2: 60.452m
DY: -899.97u

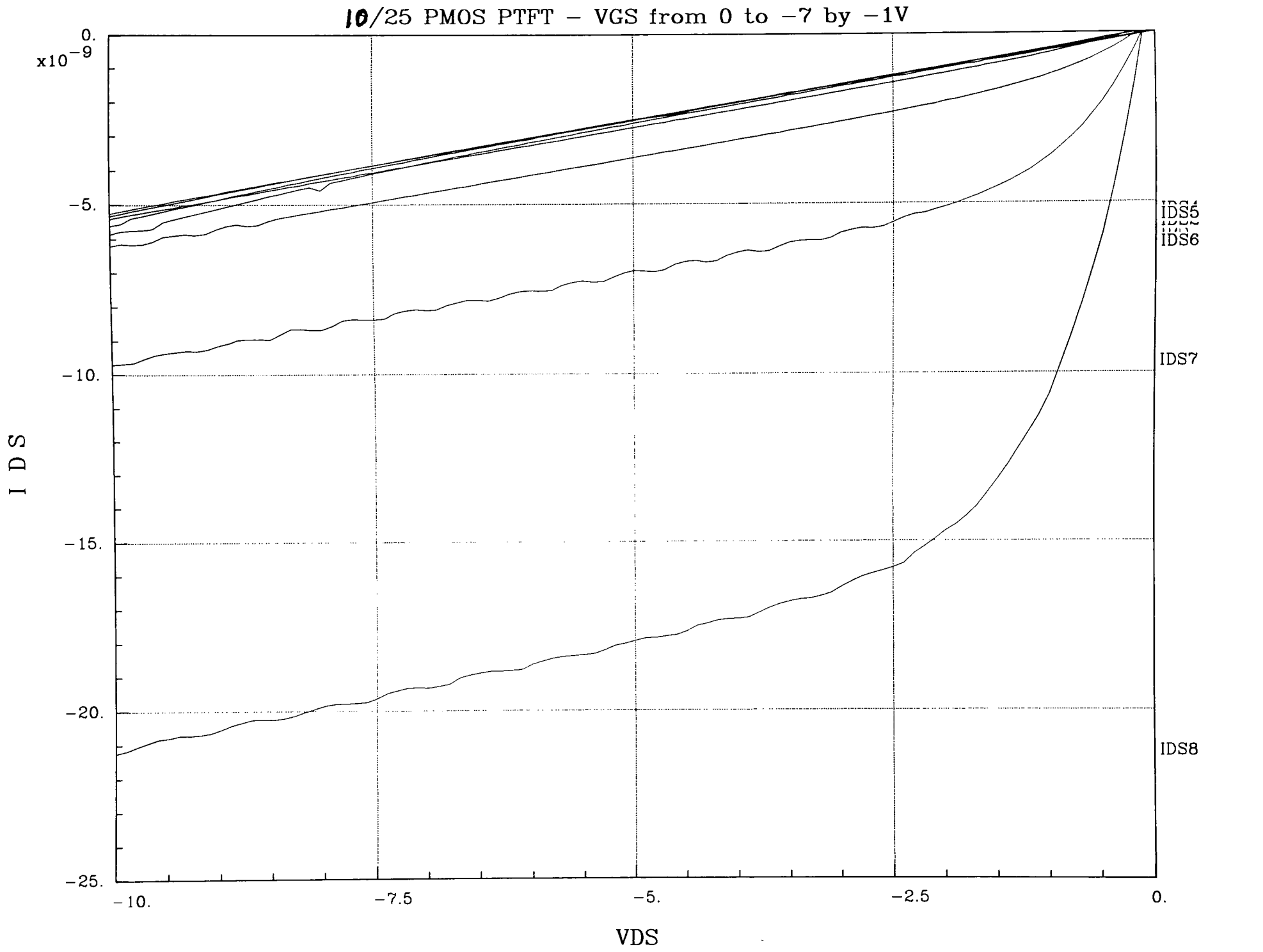
Slope: -3.750m
Y-int: 47.852m
X-int: 12.761



X1: -3.120
X2: -3.360
DX: 240.00m

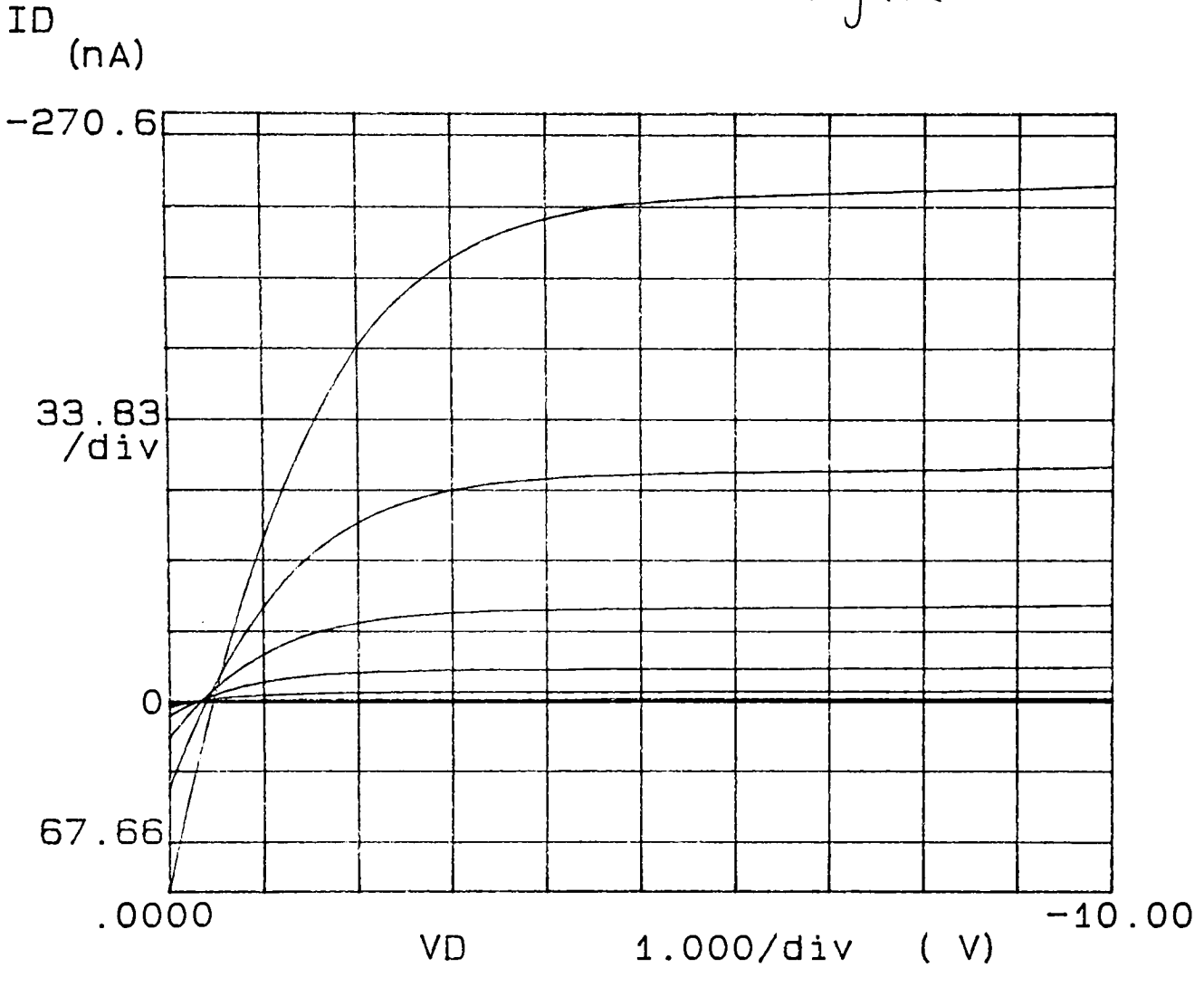
PMOS/NMOS POLYTFTs

Device Parameter Extraction Curves


10/25 PMOS PTFT – VGS from 0 to −7 by −1V
0.
x10−9
−5.
−10.
−15.
−20.
−25.
I D S
IDS4
IDS5
IDS6
IDS7
IDS8
−10.
−7.5
−5.
−2.5
0.
VDS

****** GRAPHICS PLOT ******

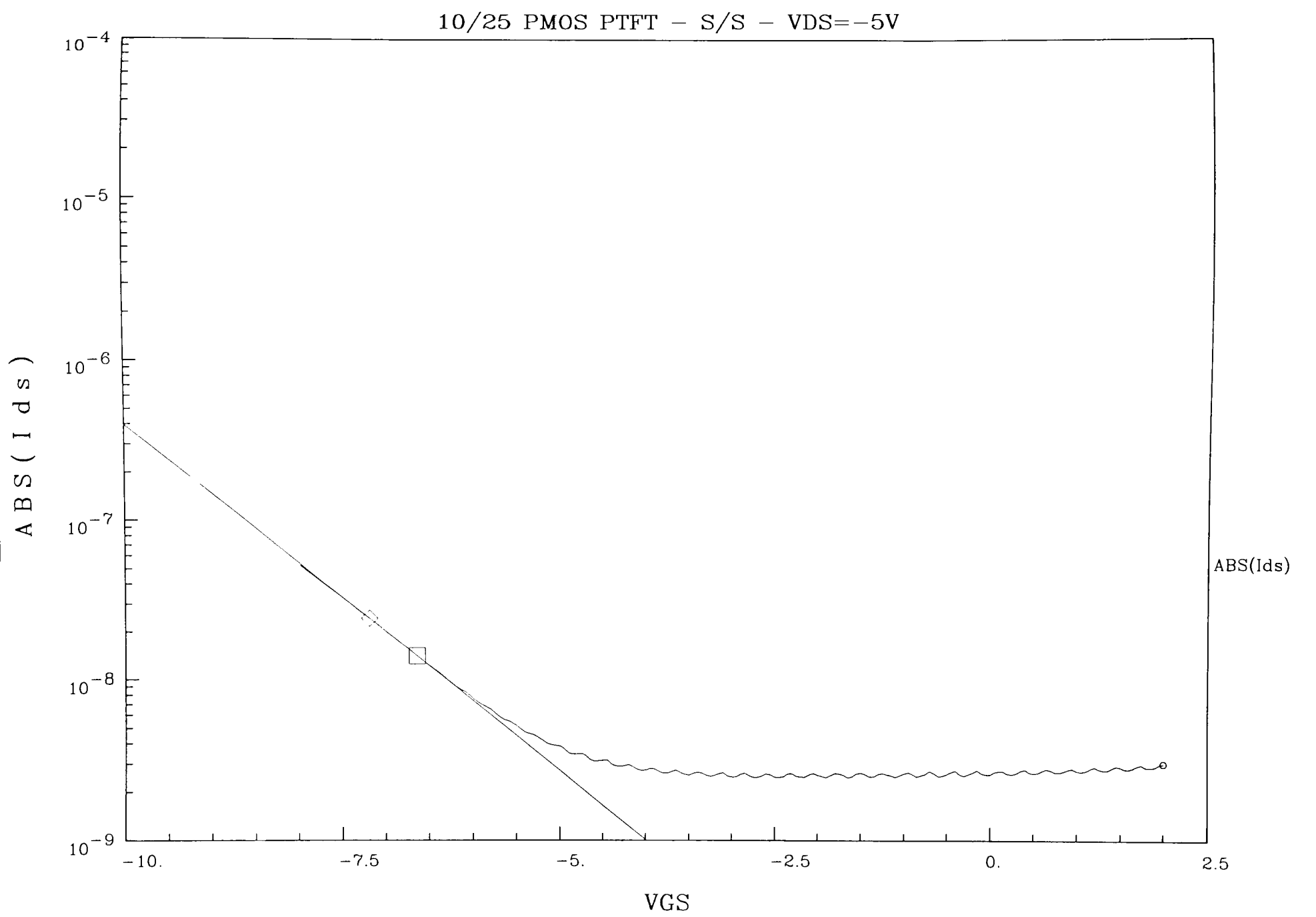
PMOS 10/10 Poly TFz



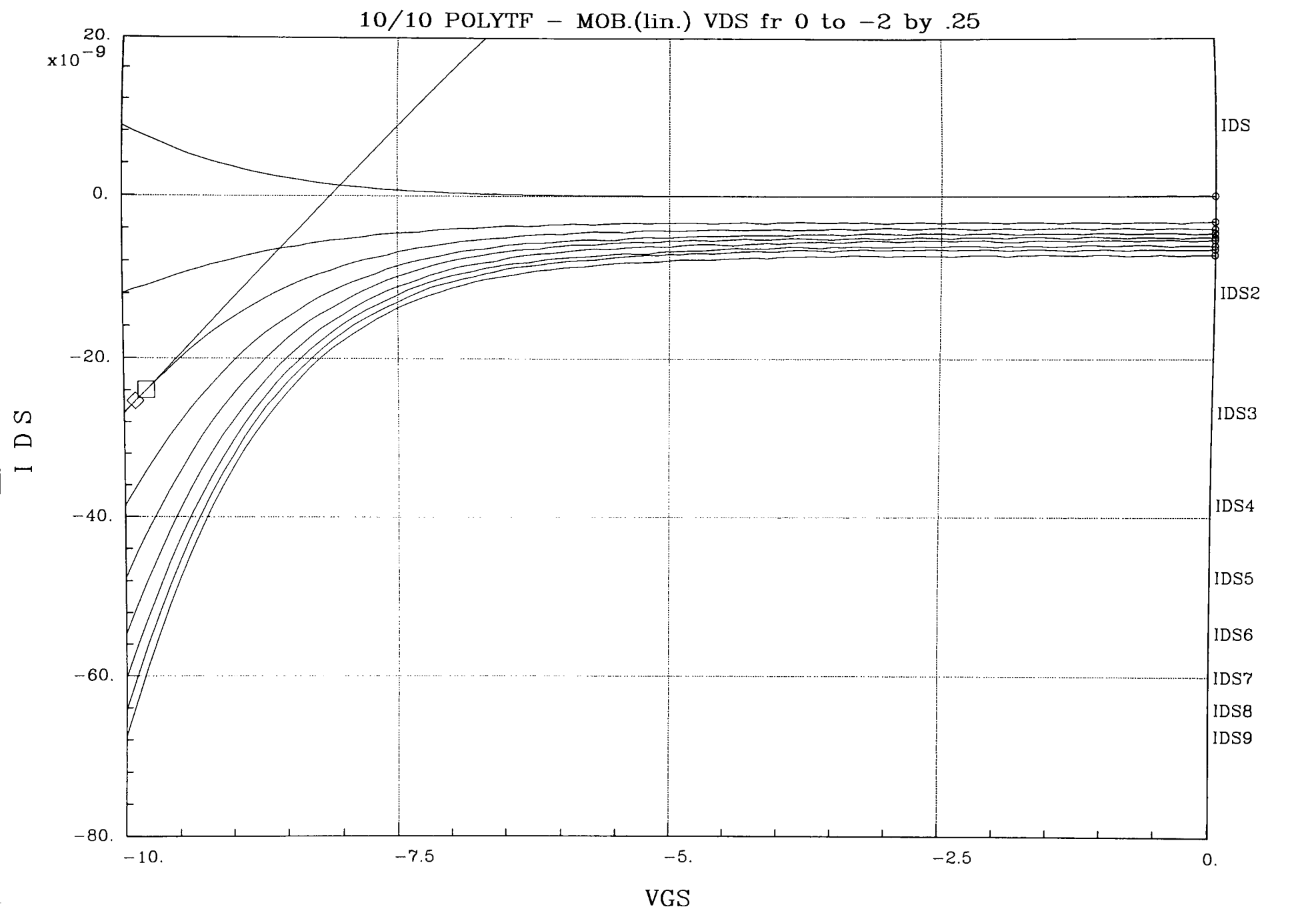
Variable1:
VD -Ch3
Linear sweep
Start .0000
Stop -10.000
Step - .2000

Variable2:
VG -Ch2
Start .0000V
Stop -11.000V
Step -1.0000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V



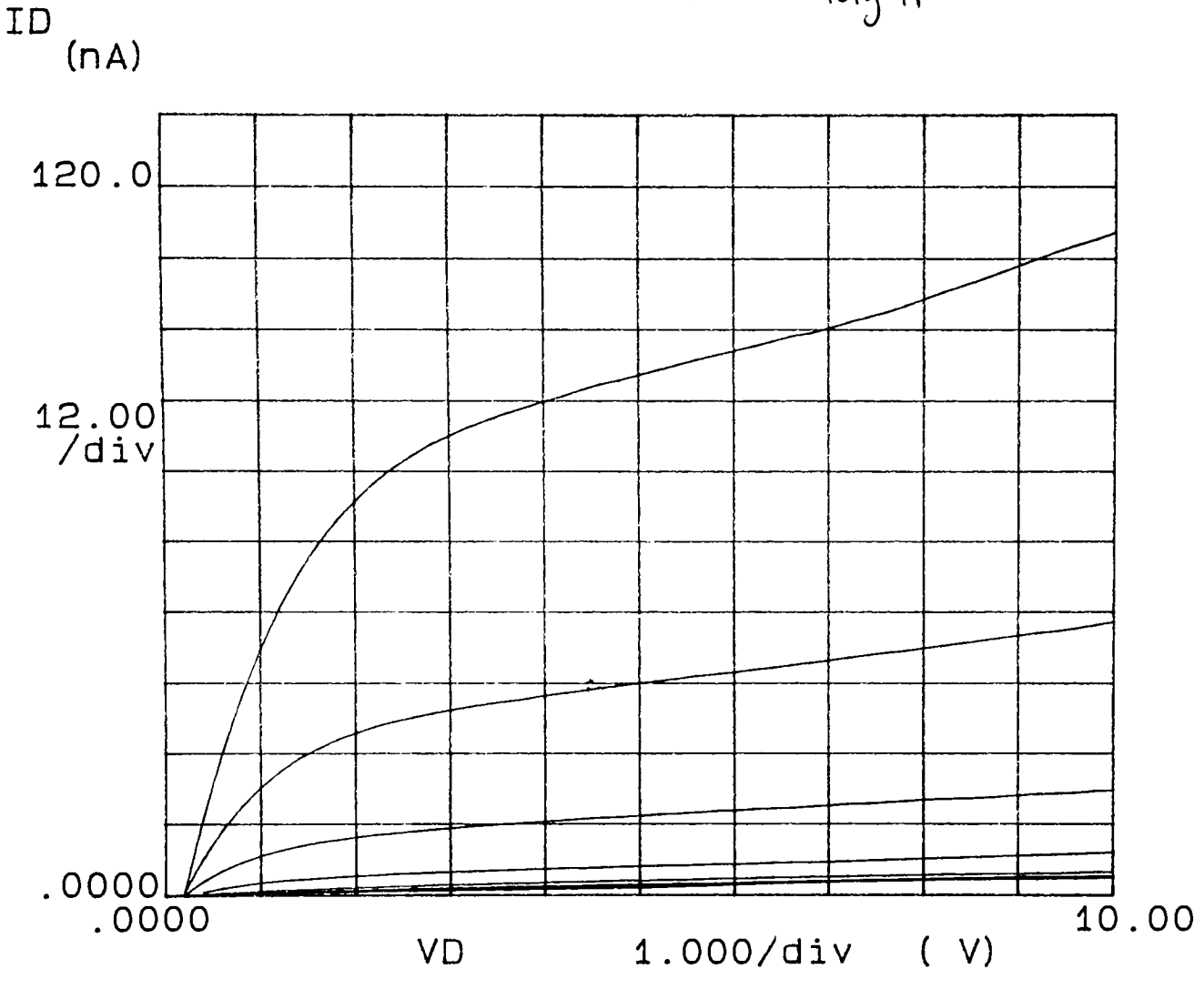
X1: –6.6500 Y1: 14.074n A: 18.77p
X2: –7.200 Y2 24.334n B: –995.5m
DX: 550.0m DY: –10.26n y = A*e~(B*x)



X1: −9.8000 Y1: −23.960n Slope: 14.150n
X2: −9.900 Y2: −25.374n Y−int: 114.71n
DX 100.00m DY: 1.415n X−int: −8.1068

****** GRAPHICS PLOT ******

NMOS 10/10 poly 4 2



Variable1:
VD -Ch3
Linear sweep
Start .0000V
Stop 10.000V
Step .2000V

Variable2:
VG -Ch2
Start .0000V
Stop 7.0000V
Step 1.0000V

Constants:
VS -Ch1 .0000V
VB -Ch4 .0000V